Hi-Flex AMIBIOS

for the

OPTi 82C495XLC

Chipset

User's Guide

Based on the 08/08/93 core AMIBIOS.
Use with AMIBCP Version 2.1a.

MANOP495XLC
12/2/93

American Megatrends, Inc.
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Revision History

12/2/93	Initial release.

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Preface

To the OEM Reader

The Hi-Flex AMIBIOS is a state of the art product which includes major engineering innovations. The Hi-Flex AMIBIOS can be easily configured by the OEM, system integrator, or VAR building systems that include the AMIBIOS through the AMIBIOS Configuration Program (AMIBCP). See the *AMIBCP User's Guide* for detailed information. This manual was written for the OEM to assist in the proper use of AMIBIOS Setup. This manual is not meant to be read by the computer owner who purchases a computer with the AMIBIOS. It is assumed that the computer manufacturer will use this manual as a sourcebook of information, and that parts of this manual will be included in the computer owner's manual. It is also assumed that the OEM, VAR, or system integrator that is reading this manual has also licensed the right to use the AMIBIOS technical documentation.

Technical Support

If an AMIBIOS fails to operate as described or you need more information, call technical support at 404-246-8600. Make sure you have the following information before calling:

- Serial number and revision number of the BIOS
- System BIOS reference number
- A clear description of the problem.

Acknowledgments

This manual was written and edited by Paul Narushoff and Robert Cheng. The writers gratefully acknowledge the assistance of the BIOS engineers.

BIOS File

This manual documents AMIBIOS files O495XLCE.ROM and O495XLCP.ROM.

Chapter 1

Introduction

This manual documents the AMIBIOS for the OPTi 82C495XLC Chipset. This chipset supports systems with the Intel 386, 486 or equivalent microprocessor, such as the Cyrix CPUs. Please see the OPTi technical documentation for additional information. The 08/08/93 core AMIBIOS used with this AMIBIOS provides many new features, including support for the power management features incorporated in the EPA Green PC specifications. See the *American Megatrends Hi-Flex ISA and EISA AMIBIOS User's Guide for the 08/08/93 core AMIBIOS* for additional information.

OPTi 82C495XLC Chipset Features

- supports CPUs operating at speeds of from 16 MHz to 33 MHz,
- supports write-back cache memory sizes of 32 KB, 64 KB, 128 KB, 256K, and 512 KB,
- supports up to 16 MB of onboard system RAM in various combinations of 256 KB x 9, 1 MB x 9, and 4 MB x 9 SIMMs (Single Inline Memory Modules).

System BIOS

The BIOS is the basic input output system used in all IBM® PC-, XT™-, AT®-, and PS/2®- compatible computers. The Hi-Flex AMIBIOS is a high-quality example of a system BIOS.

Configuration Data

AT-Compatible systems, also called ISA (Industry Standard Architecture) systems, and EISA (Extended Industry Standard Architecture) systems must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-Compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock and many systems have 128 bytes.

How Data Is Configured

The AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup is used to set configuration data in CMOS RAM.

Types of AMIBIOS Setup

Types of Setup	Description
STANDARD CMOS SETUP	Sets time, date, hard disk type, types of floppy drives, monitor type, and if keyboard is installed. These options are documented in the *Hi-Flex AMIBIOS User's Guide*.
ADVANCED CMOS SETUP	Sets Typematic Rate and Delay, Above 1 MB Memory Test, Memory Test Tick Sound, Hit <Del> Message Display, System Boot Up Sequence, and many others. These options are documented in the *Hi-Flex AMIBIOS User's Guide*.
ADVANCED CHIPSET SETUP	Sets chipset-specific options and features. The ADVANCED CHIPSET SETUP options for this AMIBIOS are described on pages through .
Peripheral Setup	Controls Peripheral-related options. Not present in

	this AMIBIOS.
Power Management Setup	Controls power conservation options. See pages through .

Features

ADVANCED BIOS Features

The ROM file for this AMIBIOS does not implement the Clock Switching, Cache Control, Turbo Switch Input Pin, or Reset Memory Controller AMIBCP options.

BIOS Information

The following graphic shows the AMIBCP BIOS Information.

BIOS Options

The following graphic illustrates the AMIBCP BIOS Options for this AMIBIOS file.

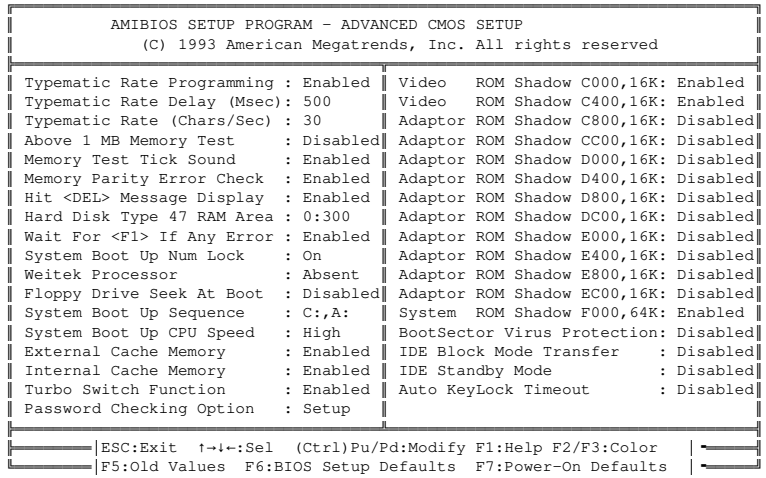
Miscellaneous BIOS Features

The following screen shows the AMIBCP Miscellaneous options for this BIOS file.

Chapter 2

ADVANCED CMOS SETUP

The ADVANCED CMOS SETUP screen is shown below. Press the →, ←, ↑, and ↓ keys to scroll through the options.



The following options are not shown above because they are marked *Absent* in AMIBCP:

Mouse Support Option,
Numeric Processor Test,
Fast Gate A20 Option,
Shadow RAM Option, *(duplicates the function of the Video ROM and System ROM options),*
Video ROM Shadow, and
CPU Internal Clock Mode.

All of the above options are described in the *Hi-Flex AMIBIOS User's Guide*. The **Fast Gate A20 Option** is marked *Absent* in AMIBCP because it is not supported by the chipset.

If No Cache Memory

If there is no cache memory on the system, use AMIBCP to disable cache memory. AMIBIOS will not report that cache memory is

not present in the system.

Default Settings

Every option in AMIBIOS Setup contains two default values: a power-on default and the BIOS Setup default value.

The Power-On Defaults

The Power-On default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

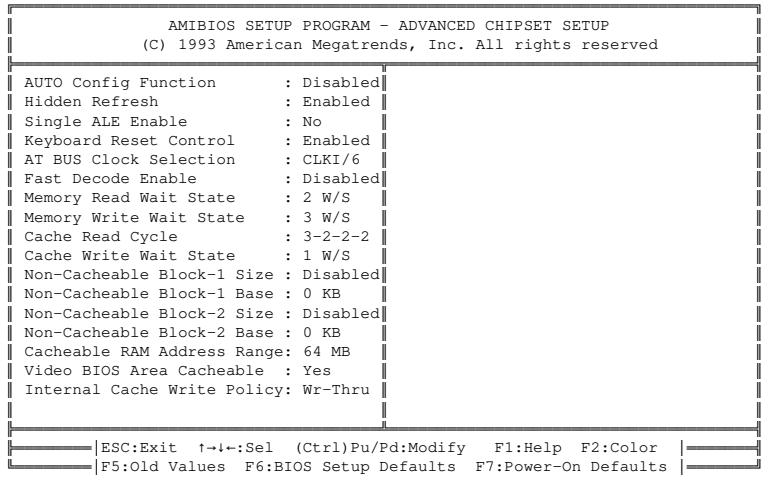
BIOS Setup Defaults

The BIOS Setup default values provide optimum performance settings for all devices and system features.

Chapter 3

ADVANCED CHIPSET SETUP

The ADVANCED CHIPSET SETUP screen is shown below. Press the →, ←, ↑, and ↓ keys to scroll through the options. See the OPTi technical documentation for additional information.



If No Cache Memory

If there is no cache memory on the system, use AMIBCP to disable cache memory. AMIBIOS will not report that cache memory is not present in the system.

Default Settings

Every option in AMIBIOS Setup contains two default values: a Power-On default and the BIOS Setup default value.

The Power-On Defaults

The Power-On default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

BIOS Setup Defaults

The BIOS Setup default values provide optimum performance settings for all devices and system features.

ADVANCED CHIPSET SETUP Options

Configuring ADVANCED CHIPSET SETUP Options

You can choose the options that are included in the ADVANCED CHIPSET SETUP via AMIBCP. See the *AMIBCP User's Guide* for additional information.

AUTO Config Function

When enabled, this option permits AMIBIOS to automatically configure ADVANCED CHIPSET SETUP options to optimal settings, based on the CPU and motherboard frequency. The settings are *Enabled* or *Disabled.* The BIOS Setup and Power-On defaults are *Disabled.*

Hidden Refresh

If this option is enabled, system DRAM memory will be refreshed without holding the CPU. This improves system performance. This option should be disabled on 80386-based systems when memory caching support is disabled. The settings are *Enabled* or *Disabled*. The BIOS Setup default is *Enabled.* The Power-On default is *Disabled*.

Single ALE Enable

If this option is enabled, SYNC will activate Single ALE instead of multiple ALEs during the bus conversion cycle. The settings are *Yes* or *No*. The BIOS Setup and Power-On defaults are *No*.

Keyboard Reset Control

If this option is enabled, a HALT instruction is executed before SYNC generates a CPU reset from a keyboard reset. The BIOS Setup default is *Enabled.* The Power-On default is *Disabled*.

AT BUS Clock Selection

This option sets the source for the AT Bus clock. The settings are *CLKI/6, CLKI/4, CLKI/3*, or *CLKI/2.5*. The BIOS Setup and Power-On defaults are *CLKI/6*.

Fast Decode Enable

The settings are *Enabled* or *Disabled*. The BIOS Setup and Power-On defaults are *Disabled*.

Memory Read Wait State

This option sets the number of wait states inserted before DRAM system memory read operations. The settings are *0 W/S, 1 W/S,* or *2 W/S*. The BIOS Setup and Power-On defaults are *2 W/S*.

Memory Write Wait State

This option sets the number of wait states inserted before DRAM system memory write operations. The settings are *0 W/S, 1 W/S, 2 W/S*, or *3 W/S*. The BIOS Setup and Power-On defaults are *3 W/S*.

Cache Read Cycle

If *3-2-2-2* or *2-2-2-2* is selected, the cache memory buffer output is disabled. The settings are *3-1-1-1, 2-2-2-2,* or *3-2-2-2.* The BIOS Setup and Power-On default is *3-2-2-2.*

Cache Write Wait State

This option sets the number of wait states inserted before all write operations to secondary (external) cache memory. The settings are *0 W/S, 1 W/S,* or *2 W/S.* The BIOS Setup and Power-On defaults are *1 W/S.*

Non-Cacheable Block-1 Size
Non-Cacheable Block-2 Size

These options define the size of two regions of memory (Block-1 and/or Block-2) whose contents cannot be read from or written to cache memory. The settings are *64 KB, 128 KB, 256 KB, 512 KB,* or *Disabled.* The BIOS Setup and Power-On defaults are *Disabled.*

Non-Cacheable Block-1 Base
Non-Cacheable Block-2 Base

These options define the base address or starting point of two regions of memory whose contents cannot be read from or written to cache memory. The base address changes in increments equal to the corresponding **Non-Cacheable Block-*x* Size**. If the setting of the **Non-Cacheable Block-*x* Size** option is *Disabled,* the only choice for the corresponding base address is *0 KB.* The BIOS Setup and Power-On defaults are *0 KB.*

Cacheable RAM Address Range

This option sets the amount of system memory that can be written to or read from cache memory. The setting cannot be greater than the total amount of system RAM. The settings are *4 MB, 8 MB, 12 MB, 16 MB, 20 MB, 24 MB, 28 MB, 32 MB, 36 MB, 40 MB, 44 MB, 48 MB, 52 MB, 56 MB, 60 MB*, or *64 MB*. The BIOS Setup and Power-On defaults are *64 MB.*

Video BIOS Area Cacheable

If this option is enabled, the contents of the video BIOS shadow RAM area (C0000h - C7FFFh) can be read from or written to cache memory, which enhances video performance. This option may be enabled only when *Video BIOS Shadowing* is enabled in ADVANCED CMOS SETUP. Before enabling this option (selecting *Yes*), you must be reasonably certain that no application will write to the video BIOS memory area while this option is enabled. The settings are *Yes* or *No*. The BIOS Setup default is *Yes.* The Power-On default is *No*.

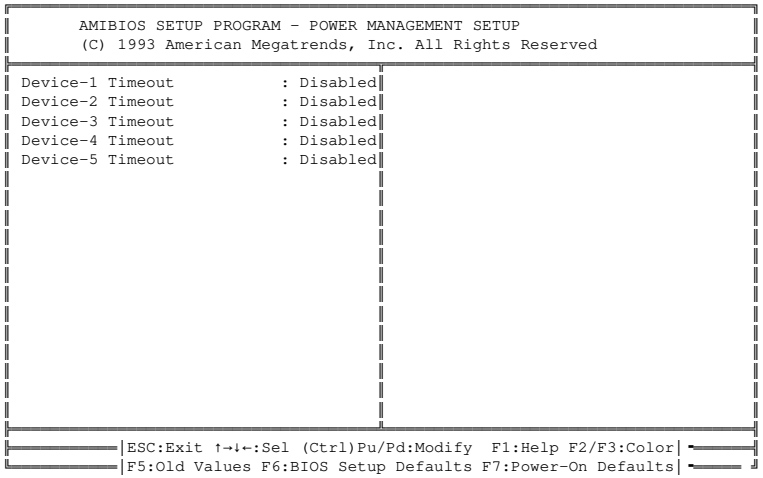
Internal Cache Write Policy

This option specifies the type of caching algorithm used by AMIBIOS. The settings are *Wr-Thru* (write-through) or *Wr-Back* (write-back). The BIOS Setup and Power-On defaults are *Wr-Thru.*

Chapter 4

Power Management Setup

The Power Management Setup screen is shown below. The Power Management Setup screen is shown below. Press the →, ←, ↑, and ↓ keys to scroll through the options.



Power Management Setup Options

Device-1 Timeout

This option is marked *Absent* in AMIBCP. This option sets the length of the Sleep mode timeout period for "Device-1". The character string "Device-1" should be replaced by the OEM in AMIBCP with a character string that represents the actual device (for example, hard disk driver, floppy drive, LCD screen). The Device-1 timeout period is the length of time with no keyboard, mouse, COM1, or COM2 activity. At the expiration of this period, AMIBIOS takes the system to Green PC Sleep Mode. The settings for this option can vary from system to system depending on the type of device. On most systems, the settings are *Disabled, 1 Min., 2 Min., 3 Min., 4 Min., 5 Min., 6 Min., 7 Min., 8 Min., 9 Min., 10 Min., 11 Min., 12 Min., 13 Min.,* or *15 Min.* The BIOS Setup and Power-On defaults are *Disabled.*

Device-2 Timeout

This option is marked *Absent* in AMIBCP. This option sets the length of the Sleep mode timeout period for "Device-2". The character string "Device-2" should be replaced by the OEM in AMIBCP with a character string that represents the actual device (for example, hard disk driver, floppy drive, LCD screen). The Device-2 timeout period is the length of time with no keyboard, mouse, COM1, or COM2 activity. At the expiration of this period, AMIBIOS takes the system to Green PC Sleep Mode. The settings for this option can vary from system to system depending on the type of device. On most systems, the settings are *Disabled, 1 Min., 2 Min., 3 Min., 4 Min., 5 Min., 6 Min., 7 Min., 8 Min., 9 Min., 10 Min., 11 Min., 12 Min., 13 Min.,* or *15 Min.* The BIOS Setup and Power-On defaults are *Disabled.*

Device-3 Timeout

This option is marked *Absent* in AMIBCP. This option sets the length of the Sleep mode timeout period for "Device-3". The character string "Device-3" should be replaced by the OEM in AMIBCP with a character string that represents the actual device (for example, hard disk driver, floppy drive, LCD screen). The Device-3 timeout period is the length of time with no keyboard, mouse, COM1, or COM2 activity. At the expiration of this period, AMIBIOS takes the system to Green PC Sleep Mode. The settings for this option can vary from system to system depending on the type of device. On most systems, the settings are *Disabled, 1 Min., 2 Min., 3 Min., 4 Min., 5 Min., 6 Min., 7 Min., 8 Min., 9 Min., 10 Min., 11 Min., 12 Min., 13 Min.,* or *15 Min.* The BIOS Setup and Power-On defaults are *Disabled.*

Device-4 Timeout

This option is marked *Absent* in AMIBCP. This option sets the length of the Sleep mode timeout period for "Device-4". The character string "Device-4" should be replaced by the OEM in AMIBCP with a character string that represents the actual device (for example, hard disk driver, floppy drive, LCD screen). The Device-4 timeout period is the length of time with no keyboard, mouse, COM1, or COM2 activity. At the expiration of this period, AMIBIOS takes the system to Green PC Sleep Mode. The settings for this option can vary from system to system depending on the type of device. On most systems, the settings are *Disabled, 1 Min., 2 Min., 3 Min., 4 Min., 5 Min., 6 Min., 7 Min., 8 Min., 9 Min., 10 Min., 11 Min., 12 Min., 13 Min.,* or *15 Min.* The BIOS Setup and Power-On defaults are *Disabled.*

Device-5 Timeout

This option is marked *Absent* in AMIBCP. This option sets the length of the Sleep mode timeout period for "Device-5". The character string "Device-5" should be replaced by the OEM in AMIBCP with a character string that represents the actual device (for example, hard disk driver, floppy drive, LCD screen). The Device-5 timeout period is the length of time with no keyboard, mouse, COM1, or COM2 activity. At the expiration of this period, AMIBIOS takes the system to Green PC Sleep Mode. The settings for this option can vary from system to system depending on the type of device. On most systems, the settings are *Disabled, 1 Min., 2 Min., 3 Min., 4 Min., 5 Min., 6 Min., 7 Min., 8 Min., 9 Min., 10 Min., 11 Min., 12 Min., 13 Min.,* or *15 Min.* The BIOS Setup and Power-On defaults are *Disabled.*

Chapter 5

CMOS RAM Map

A map of CMOS RAM as configured by the AMIBIOS for the OPTi 82C495XLC chipset is shown in the following table.

Offset	Description
00h - 0Fh	Standard IBM AT compatible RTC and Status Register data definitions.
10h	Floppy Drive Type Bits 7-4 Drive A: Type 0 No Drive 1 360 KB Drive 2 1.2 MB Drive 3 720 KB Drive 4 1.44 MB Drive 5 2.88 MB Drive Bits 3-0 Drive B: Type (bit settings same as A)
11h	Bit 7 Mouse Support Option (1 = Enabled) Bit 6 Above 1 MB Memory Test (1 = Enabled) Bit 5 Memory Test Tick Sound (1 = Enabled) Bit 4 Memory Parity Error Check (1 = Enabled) Bit 3 Hit <DEL> Message Display (1 = Enabled) Bit 2 Hard Disk Type 47 RAM Area (1 = 0:300h) Bit 1 Wait for <F1> if Any Error (1 = Enabled) Bit 0 System Boot Up Num Lock (1 = On)
12h	Hard Disk Data Bits 7-4 Hard Disk Drive C: Type 0 No drive 1-14 Hard drive Type 1-14 16 Hard Disk Type 16-255 (actual Hard Drive Type is in CMOS RAM 1Ah) Bits 3-0 Hard Disk Drive D: Type (Same as C:)
13h	Bit 7 Typematic Rate Programming (1 = Enabled) Bits 6-5 Typematic Delay (in milliseconds) 00 250 ms 01 500 ms 10 750 ms 11 100 ms Bits 4-2 Typematic Rate (Characters per second) 000 6 cps 001 8 cps

	010 10 cps 011 12 cps 100 15 cps 101 20 cps 110 24 cps 111 30 cps
14h	Equipment Byte Bits 7-6 Number of Floppy Drives 00 1 Drive 01 2 Drives Bits 5-4 Monitor Type 00 Not CGA or MDA 01 40x25 CGA 10 80x25 CGA 11 MDA (Monochrome) Bit 3 Display Enabled (1 = Enabled) Bit 2 Keyboard Enabled (1 = Enabled) Bit 1 Math coprocessor Installed (1 = Enabled) Bit 0 Floppy Drive Installed (0 = Enabled)
15h	Base Memory (in 1 KB increments), Low Byte
16h	Base Memory (in 1 KB increments), High Byte
17h	Extended Memory (in 1 KB increments), Low Byte
18h	Extended Memory (in 1 KB increments), High Byte (Max 15 MB)
19h	Hard Disk C: Drive Type 0-15 Reserved 16-255 Hard Drive Type 16-255
1Ah	Hard Disk D: Drive Type (Same as Drive C: above)
1Bh	User-Defined Drive C: - # of Cylinders, Low Byte
1Ch	User-Defined Drive C: - # of Cylinders, High Byte
1Dh	User-Defined Drive C: - Number of Heads
1Eh	User-Defined Drive C: - Write Precompensation Cylinder, Low Byte
1Fh	User-Defined Drive C: - Write Precompensation Cylinder, High Byte
20h	User-Defined Drive C: - Control Byte (80h if # of heads is equal or greater than 8)
21h	User-Defined Drive C: - Landing Zone, Low Byte
22h	User-Defined Drive C: - Landing Zone, High Byte
23h	User-Defined Drive C: - # of Sectors
24h	User-Defined Drive D: - # of Cylinders, Low Byte

25h	User-Defined Drive D: - # of Cylinders, High Byte
26h	User-Defined Drive D: - Number of Heads
27h	User-Defined Drive D: - Write Precompensation Cylinder, Low Byte
28h	User-Defined Drive D: - Write Precompensation Cylinder, High Byte
29h	User-Defined Drive D: - Control Byte (80h if # of heads is equal or greater than 8)
2Ah	User-Defined Drive D: - Landing Zone, Low Byte
2Bh	User-Defined Drive D: - Landing Zone, High Byte
2Ch	User-Defined Drive D: - # of Sectors
2Dh	Bit 7 Weitek Processor (1 = Present) Bit 6 Floppy Drive Seek At Boot (1 = Enabled) Bit 5 System Boot Up Sequence (1 = A:, C:) Bit 4 System Boot Up CPU Speed (1 = High) Bit 3 External Cache Memory (1 = Enabled) Bit 2 Internal Cache Memory (1 = Enabled) Bit 1 Fast Gate A20 Option (1 = Enabled) Bit 0 Turbo Switch Function (1 = Enabled)
2Eh	Standard CMOS Checksum, High Byte
2Fh	Standard CMOS Checksum, Low Byte
30h	Extended Memory, Low Byte
31h	Extended Memory, High Byte (Maximum 15 MB)
32h	Century Byte (BCD value for the century)
33h	Information Flag Bit 7 BIOS Size (1 = 128 KB) Bits 6-0 Reserved
34h	Bit 7 Boot Sector Virus Protection (1 = Enabled) Bit 6 Password 0 Always 0 Setup Bit 5 Adaptor ROM Shadow C800,16K (1 = Enabled) Bit 4 Adaptor ROM Shadow CC00,16K (1 = Enabled) Bit 3 Adaptor ROM Shadow D000,16K (1 = Enabled) Bit 2 Adaptor ROM Shadow D400,16K (1 = Enabled) Bit 1 Adaptor ROM Shadow D800,16K (1 = Enabled) Bit 0 Adaptor ROM Shadow DC00,16K (1 = Enabled)
35h	Bit 7 Adaptor ROM Shadow E000,16K (1 = Enabled) Bit 6 Adaptor ROM Shadow E400,16K (1 = Enabled)

	Bit 5 Adaptor ROM Shadow E800,16K (1 = Enabled) Bit 4 Adaptor ROM Shadow EC00,16K (1 = Enabled) Bit 3 System BIOS Shadow F000,64K (1 = Enabled) Bit 2 Video ROM Shadow C000, 16K (1 = Enabled) Bit 1 Video ROM Shadow C400,16K (1 = Enabled) Bit 0 Numeric Processor Test (1 = Enabled)
36h	Bit 7 IDE Block Mode Transfer 0 Disabled 1 Enabled Bits 6-5 CPU Internal Clock Mode 00 2X 01 1X Bit 4 IDE Standby Mode 0 Disabled 1 Enabled Bits 3-0 Auto KeyLock Timeout 0000 Disabled 0001 1 Min. 0010 2 Min. 0011 3 Min. 0100 4 Min. 0101 5 Min. 0110 6 Min. 0111 7 Min. 1000 8 Min. 1001 9 Min. 1010 10 Min. 1011 11 Min. 1100 12 Min. 1101 13 Min 1110 14 Min. 1111 15 Min.
37h	Reserved
38h - 3Dh	Encrypted Password
3Eh	Extended CMOS Checksum, High Byte (includes 34h - 3Dh)
3Fh	Extended CMOS Checksum, Low Byte (includes 34h - 3Dh)

Extended CMOS RAM

Offset	Description
40h	Bits 7-0 Device-1 Timeout
41h	Bits 7-0 Device-2 Timeout
42h	Bits 7-0 Device-3 Timeout
43h	Bits 7-0 Device-4 Timeout
44h	Bits 7-0 Device-5 Timeout
45h - 47h	Reserved
48h	Bit 1 Internal Cache Write Policy 0 Wr-Thru 1 Wr-Back
49h - 5Fh	Reserved
60h	Bit 3 Single ALE Enable 0 No 1 Yes Bit 1 Keyboard Reset Control 0 Disabled 1 Enabled
61h	Bits 6,1 Cache Write Wait State 00 1 W/S 01 0 W/S 10 2 W/S Bit 0 Cache Read Cycle
62h	Bit 2 Hidden Refresh 0 Disabled 1 Enabled
63h - 64h	Reserved
65h	Bits 7-6 Memory Read Wait State 01 0 W/S 10 1 W/S 11 2 W/S Bits 5-4 Memory Write Wait State 00 0 W/S 01 1 W/S 10 2 W/S 11 3 W/S Bit 3 Fast Decode Enable 0 Disabled 1 Enabled

	Bits 1-0 AT BUS Clock Selection 00 CLKI/6 01 CLKI/4 10 CLKI/3 11 CLKI/5
66h	Reserved
67h	Bits 4 Video BIOS Area Cacheable 0 No 1 Yes Bits 3-0 Cacheable RAM Address Range 0000 64 MB 0001 4 MB 0010 8 MB 0011 12 MB 0100 16 MB 0101 20 MB 0110 24 MB 0111 28 MB 1000 32 MB 1001 36 MB 1010 40 MB 1011 44 MB 1100 48 MB 1101 52 MB 1110 56 MB 1111 60 MB
68h	Bits 7–5 Non-Cacheable Block-1 Size 000 64 KB 001 128 KB 010 256 KB 011 512 KB 100 Disabled
69h	Bits 7-0 Non-Cacheable Block-1 Base
6Ah	Bits 7–5 Non-Cacheable Block-2 Size 000 64 KB 001 128 KB 010 256 KB 011 512 KB 100 Disabled
6Bh	Bits 7-0 Non-Cacheable Block-2 Base
6Ch - 7Fh	Reserved

Chapter 6

Chipset Registers

The AMIBIOS for the OPTi 82C495XLC chipset sets the chipset registers as follows.

Register	Description
16h	Reserved
20h	Bit 3 Single ALE Enable 0 No 1 Yes Bit 1 Keyboard Reset Control 0 Disabled 1 Enabled Bit 0 Cyrix CPU present 0 No 1 Yes
21h	Bits 6,1 Cache Write Wait State 00 1 W/S 01 0 W/S 10 2 W/S Bit 0 Cache Read Cycle
22h	Bit 2 Hidden Refresh 0 Disabled 1 Enabled
23h	Reserved
24h	Reserved
25h	Bits 7-6 Memory Read Wait State 01 0 W/S 10 1 W/S 11 2 W/S Bits 5-4 Memory Write Wait State 00 0 W/S 01 1 W/S 10 2 W/S 11 3 W/S Bit 3 Fast Decode Enable 0 Disabled 1 Enabled Bits 1-0 AT BUS Clock Selection 00 CLKI/6 01 CLKI/4 10 CLKI/3 11 CLKI/5
26h	Reserved

27h	Bit 4 Video BIOS Area Cacheable 0 Yes 1 No Bits 3-0 Cacheable RAM Address Range 0000 64 MB 0001 4 MB 0010 8 MB 0011 12 MB 0100 16 MB 0101 20 MB 0110 24 MB 0111 28 MB 1000 32 MB 1001 36 MB 1010 40 MB 1011 44 MB 1100 48 MB 1101 52 MB 1110 56 MB 1111 60 MB
28h	Bits 7-5 Non-Cacheable Block-1 Size 000 64 KB 001 128 KB 010 256 KB 011 512 KB 100 Disabled
29h	Bits 7-0 Non-Cacheable Block-1 Base
2Ah	Bits 7-5 Non-Cacheable Block-1 Size 000 64 KB 001 128 KB 010 256 KB 011 512 KB 100 Disabled
2Bh	Bits 7-0 Non-Cacheable Block-1 Base
2Ch	Bit 0 AUTO Config Function 0 Disabled 1 Enabled
2Dh - 2Eh	Reserved
40h	Bits 7-0 Device-1 Timeout
41h	Bits 7-0 Device-2 Timeout
42h	Bits 7-0 Device-3 Timeout
43h	Bits 7-0 Device-4 Timeout
44h	Bits 7-0 Device-5 Timeout

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