



Frequency Generator & Integrated Buffers for PENTIUM/Pro™

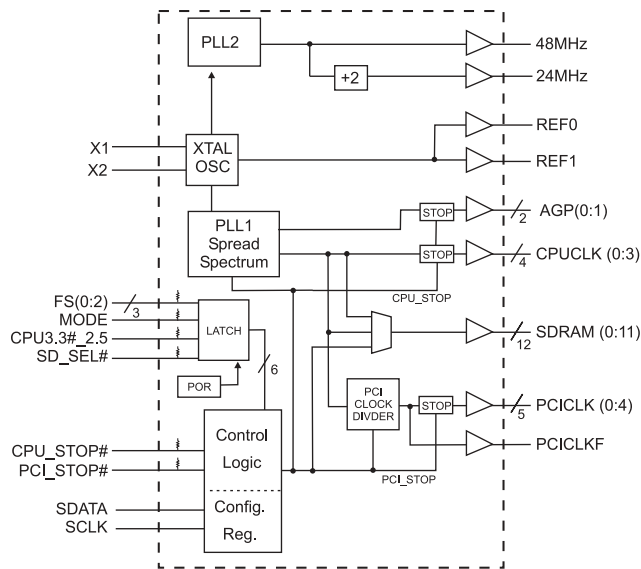
General Description

The **ICS9148-37** is the single chip clock solution for Desktop/Notebook designs using the VIA MVP3 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9148-37** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I²C interface allows changing functions, stop clock programming and frequency selection. The SD_SEL latched input allows the SDRAM frequency to follow the CPUCLK frequency (SD_SEL=1) or the AGP clock frequency (SD_SEL=0)

Block Diagram



Power Groups

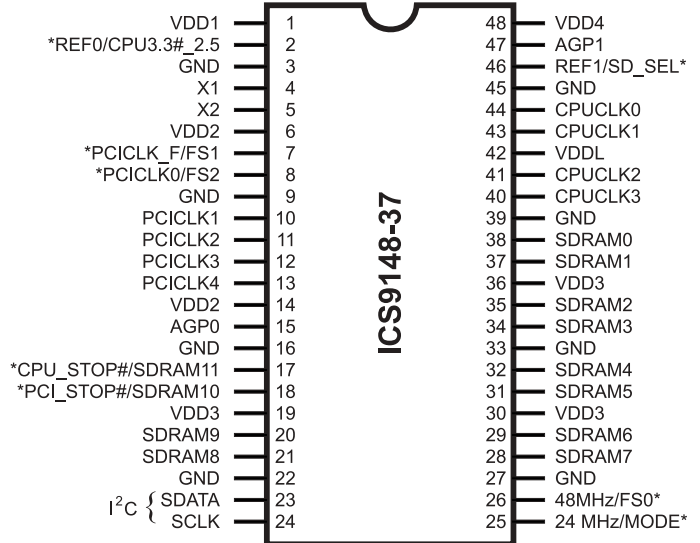
- VDD1 = REF (0:1), X1, X2
- VDD2 = PCICLK_F, PCICLK(0:5)
- VDD3 = SDRAM (0:11), supply for PLL core, 24 MHz, 48MHz
- VDD4 = AGP (0:1)
- VDDL = CPUCLK (0:3)

0143G—08/04/04

Features

- Generates the following system clocks:
 - 4 CPU(2.5V/3.3V) upto 100MHz.
 - 6 PCI(3.3V) @ 33.3MHz
 - 2AGP(3.3V) @ 2 x PCI
 - 12 SDRAMs(3.3V) @ either CPU or AGP
 - 2 REF (3.3V) @ 14.318MHz
- Skew characteristics:
 - CPU – CPU ≤ 250ps
 - SDRAM – SDRAM ≤ 250ps
 - CPU – SDRAM ≤ 250ps
 - CPU-AGP: ≤ 1ns
 - CPU(early) – PCI : 1-4ns
- Supports Spread Spectrum modulation ±0.25, ±0.6%
- Serial I²C interface for Power Management, Frequency Select, Spread Spectrum.
- Efficient Power management scheme through PCI and CPU STOP CLOCKS.
- Uses external 14.318MHz crystal
- 48 pin 300mil SSOP.

Pin Configuration



48-Pin SSOP

* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|-------------------------------------|----------------------------|------|---|
| 1 | VDD1 | PWR | Ref (0:2), XTAL power supply, nominal 3.3V |
| 2 | REF0 | OUT | 14.318 MHz reference clock. |
| | CPU3.3#_2.5 ^{1,2} | IN | Indicates whether VDDL2 is 3.3V or 2.5V. High=2.5V CPU, LOW=3.3V CPU ¹ . Latched input ² |
| 3,9,16,22,27,33,39,45 | GND | PWR | Ground |
| 4 | X1 | IN | Crystal input, has internal load cap (33pF) and feedback resistor from X2 |
| 5 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (33pF) |
| 6,14 | VDD2 | PWR | Supply for PCICLK_F and PCICLK (0:5), nominal 3.3V |
| 7 | PCICLK_F | OUT | Free running PCI clock output. Synchronous with CPUCLKs with 1-4ns skew (CPU early) This is not affected by PCI_STOP# |
| | FS ^{1,2} | IN | Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies. |
| 8 | PCICLK0 | OUT | PCI clock output. Synchronous CPUCLKs with 1-4ns skew (CPU early) |
| | FS ^{2,1,2} | IN | Frequency select pin. Latched Input Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies. |
| 10, 11, 12, 13 | PCICLK(1:4) | OUT | PCI clock outputs. Synchronous CPUCLKs with 1-4ns skew (CPU early) |
| 15, 47 | AGP (0:1) | OUT | Advanced Graphic Port outputs, powered by VDD4. |
| 17 | CPU_STOP# ¹ | IN | This asynchronous input halts CPUCLK (0:3) and AGP (0:1) clocks at logic 0 level, when input low (in Mobile Mode, MODE=0) |
| | SDRAM 11 | OUT | SDRAM clock output. Frequency is selected by the SD_SEL latched input. SD_SEL = 1 at power on causes SDRAM frequency = CPU frequency SD_SEL = 0 at power on causes SDRAM frequency = AGP frequency |
| 18 | PCI_STOP# ¹ | IN | This asynchronous input halts PCICLK(0:5) clocks at logic 0 level, when input low (In mobile mode, MODE=0) |
| | SDRAM 10 | OUT | SDRAM clock output. Frequency is selected by the SD_SEL latched input. SD_SEL = 1 at power on causes SDRAM frequency = CPU frequency SD_SEL = 0 at power on causes SDRAM frequency = AGP frequency |
| 20, 21,28, 29, 31, 32, 34, 35,37,38 | SDRAM (0:9) | OUT | SDRAM clock outputs. Frequency is selected by the SD_SEL latched input. SD_SEL = 1 at power on causes SDRAM frequency = CPU frequency SD_SEL = 0 at power on causes SDRAM frequencies = AGP frequency |
| 19,30,36 | VDD3 | PWR | Supply for SDRAM (0:11), CPU Core and 24, 48MHz clocks, nominal 3.3V. |
| 23 | SDATA | IN | Data input for I ² C serial input. |
| 24 | SCLK | IN | Clock input of I ² C input |
| 25 | 24MHz | OUT | 24MHz output clock, for Super I/O timing. |
| | MODE ^{1, 2} | IN | Pin 17, pin 18 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input. |
| 26 | 48MHz | OUT | 48MHz output clock, for USB timing. |
| | FS ^{0,1,2} | IN | Frequency select pin. Latched Input Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies. |
| 40, 41, 43, 44 | CPUCLK(0:3) | OUT | CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low |
| 42 | VDDL | PWR | Supply for CPU (0:3), either 2.5V or 3.3V nominal |
| 46 | REF1 | OUT | 14.318MHz reference clock. |
| | SD_SEL | IN | Latched input at Power On selects either CPU (SDSEL=1) or AGP (SD_SEL=0) frequencies for the SDRAM clock outputs. |
| 48 | VDD4 | PWR | Supply for AGP (0:1) |

Notes:

- 1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



Mode Pin - Power Management Input Control

| MODE, Pin 25 (Latched Input) | Pin 17 | Pin 18 |
|---------------------------------|----------------------|----------------------|
| 0 | CPU_STOP# (INPUT) | PCI_STOP# (INPUT) |
| 1 | SDRAM 11 (OUTPUT) | SDRAM 10 (OUTPUT) |

Power Management Functionality

| CPU_STOP# | PCI_STOP# | AGP, CPUCLK Outputs | PCICLK (0:5) | PCICLK_F, REF, 24/48MHz and SDRAM | Crystal OSC | VCO |
|-----------|-----------|---------------------------|--------------|--|----------------|---------|
| 0 | 1 | Stopped Low | Running | Running | Running | Running |
| 1 | 1 | Running | Running | Running | Running | Running |
| 1 | 0 | Running | Stopped Low | Running | Running | Running |

CPU 3.3#_2.5V Buffer selector for CPUCLK drivers.

| CPU3.3#_2.5 Input level (Latched Data) | Buffer Selected for operation at: |
|--|--------------------------------------|
| 1 | 2.5V VDD |
| 0 | 3.3V VDD |

Functionality

V_{DD1, 2, 3, 4} = 3.3V±5%, V_{DDL} = 2.5V ±5% or 3.3 ±5%, TA= 0 to 70°C
 Crystal (X1, X2) = 14.31818MHz

| FS2 | FS1 | FS0 | CPU (MHz) | SDRAM (MHz) | | PCI (MHz) | AGP (MHz) |
|-----|-----|-----|--------------|-------------|----------|-----------|-----------|
| | | | | SD_SEL=1 | SD_SEL=0 | | |
| 1 | 1 | 1 | 100 | 100 | 66.6 | 33.3 | 66.6 |
| 1 | 1 | 0 | 95.25 | 95.25 | 63.5 | 31.75 | 63.5 |
| 1 | 0 | 1 | 83.3 | 83.3 | 66.6 | 33.3 | 66.6 |
| 1 | 0 | 0 | 75 | 75 | 60 | 30 | 60 |
| 0 | 1 | 1 | 75 | 75 | 75 | 37.5 | 75 |
| 0 | 1 | 0 | 68.5 | 68.5 | 68.5 | 34.25 | 68.5 |
| 0 | 0 | 1 | 66.8 | 66.8 | 66.8 | 33.4 | 66.8 |
| 0 | 0 | 0 | 60 | 60 | 60 | 30 | 60 |



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

| How to Write: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

| Bit | Description | | | | PWD |
|---------|--|-----------|-------|------|--------|
| Bit 7 | 0 - $\pm 0.25\%$ Spread Spectrum Modulation 1 - $\pm 0.6\%$ Spread Spectrum Modulation | | | | 0 |
| Bit 6:4 | Bit6 Bit5 | CPU Clock | PCI | AGP | Note 1 |
| | Bit4 111 | 100 | 33.3 | 66.6 | |
| | 110 | 95.25 | 31.75 | 63.5 | |
| | 101 | 83.3 | 33.3 | 66.6 | |
| | 100 | 75 | 30 | 60 | |
| | 011 | 75 | 37.5 | 75 | |
| | 010 | 68.5 | 34.25 | 68.5 | |
| | 001 | 66.8 | 33.4 | 66.8 | |
| 000 | 60 | 30 | 60 | | |
| Bit 3 | 0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above) | | | | 0 |
| | 0 - Spread Spectrum center spread type. 1 - Spread Spectrum down spread type. | | | | 0 |
| Bit 1 | 0 - Normal 1 - Spread Spectrum Enabled | | | | 0 |
| Bit 0 | 0 - Running 1 - Tristate all outputs | | | | 0 |

Byte 1: CPU, Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|---------------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 40 | 1 | CPUCLK3 (Act/Inact) |
| Bit 2 | 41 | 1 | CPUCLK2 (Act/Inact) |
| Bit 1 | 43 | 1 | CPUCLK1 (Act/Inact) |
| Bit 0 | 44 | 1 | CPUCLK0 (Act/Inact) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCI Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|----------------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | 7 | 1 | PCICLK_F (Act/Inact) |
| Bit 5 | 15 | 1 | AGP0 (Act/Inact) |
| Bit 4 | 13 | 1 | PCICLK4 (Act/Inact) |
| Bit 3 | 12 | 1 | PCICLK3 (Act/Inact) |
| Bit 2 | 11 | 1 | PCICLK2 (Act/Inact) |
| Bit 1 | 10 | 1 | PCICLK1 (Act/Inact) |
| Bit 0 | 8 | 1 | PCICLK0(Act/Inact) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.


Byte 3: SDRAM Active/Inactive Register
 (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|--------------------|
| Bit 7 | 28 | 1 | SDRAM7 (Act/Inact) |
| Bit 6 | 29 | 1 | SDRAM6 (Act/Inact) |
| Bit 5 | 31 | 1 | SDRAM5 (Act/Inact) |
| Bit 4 | 32 | 1 | SDRAM4 (Act/Inact) |
| Bit 3 | 34 | 1 | SDRAM3 (Act/Inact) |
| Bit 2 | 35 | 1 | SDRAM2 (Act/Inact) |
| Bit 1 | 37 | 1 | SDRAM1 (Act/Inact) |
| Bit 0 | 38 | 1 | SDRAM0 (Act/Inact) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 5: Peripheral Active/Inactive Register
 (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|------------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 47 | 1 | AGP1 (Act/Inact) |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | 46 | 1 | REF1 (Act/Inact) |
| Bit 0 | 2 | 1 | REF0 (Act/Inact) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 4: SDRAM Active/Inactive Register
 (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|--|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 17 | 1 | SDRAM11 (Act/Inact) (Desktop Mode Only) |
| Bit 2 | 18 | 1 | SDRAM10 (Act/Inact) (Desktop Mode Only) |
| Bit 1 | 20 | 1 | SDRAM9 (Act/Inact) |
| Bit 0 | 21 | 1 | SDRAM8 (Act/Inact) |

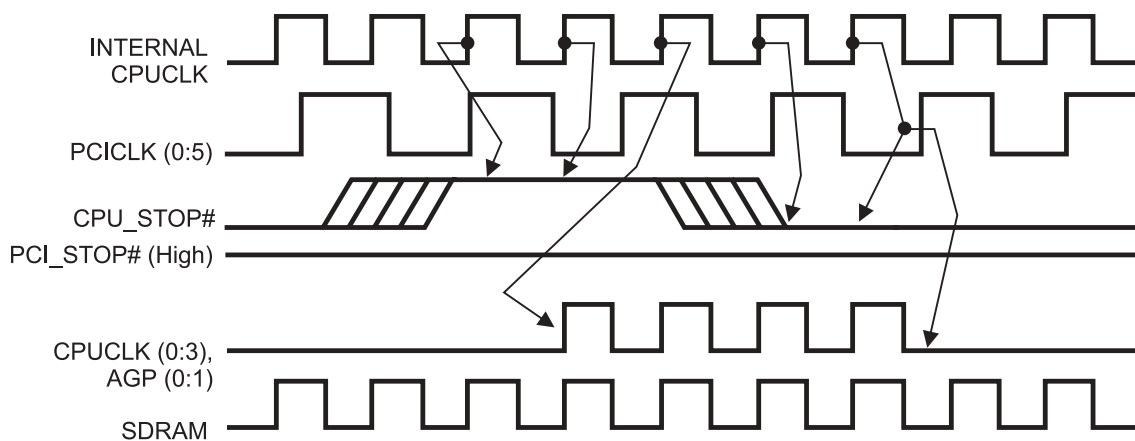
Notes:

1. Inactive means outputs are held LOW and are disabled from switching.



CPU_STOP# Timing Diagram

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the ICS9148-37. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



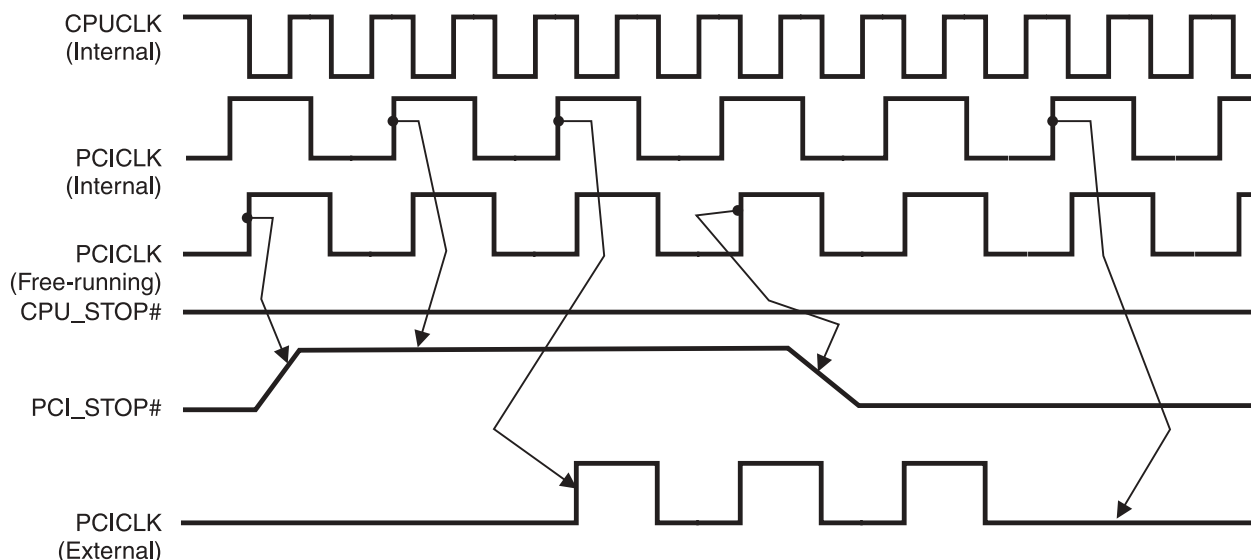
Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9148-37.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).



PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9148-37**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-37** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.



Shared Pin Operation - Input/Output Pins

Pins 2, 7, 8, 25, 26 and 46 on the **ICS9148-37** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

solder spot tabs or a physical jumper header may be used. These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either

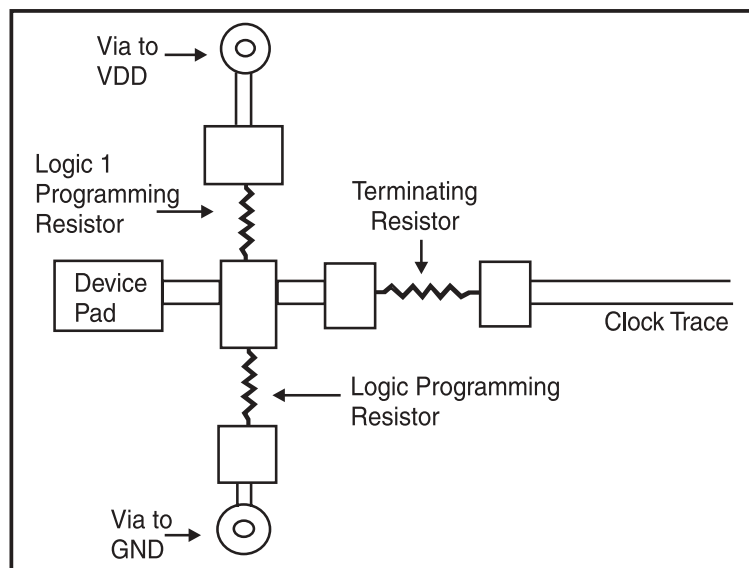


Fig. 1

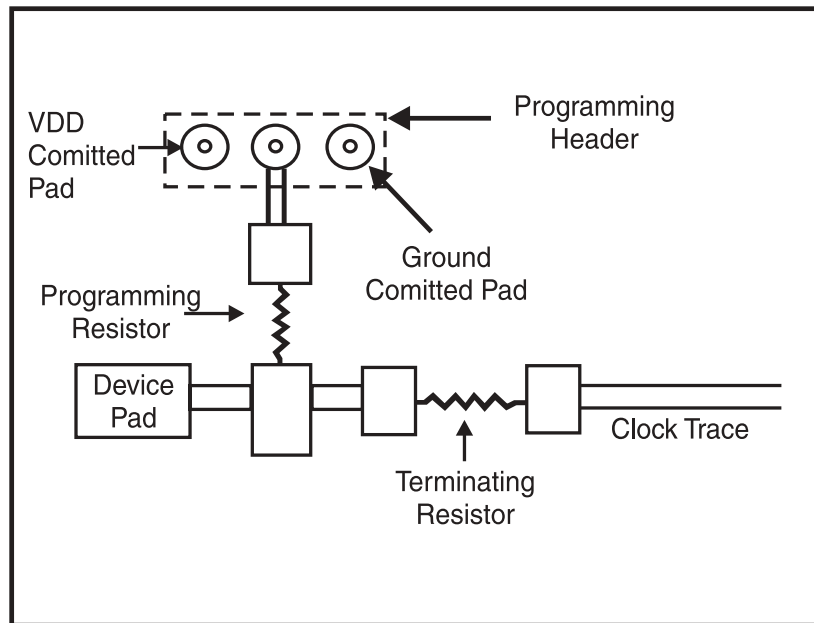


Fig. 2a

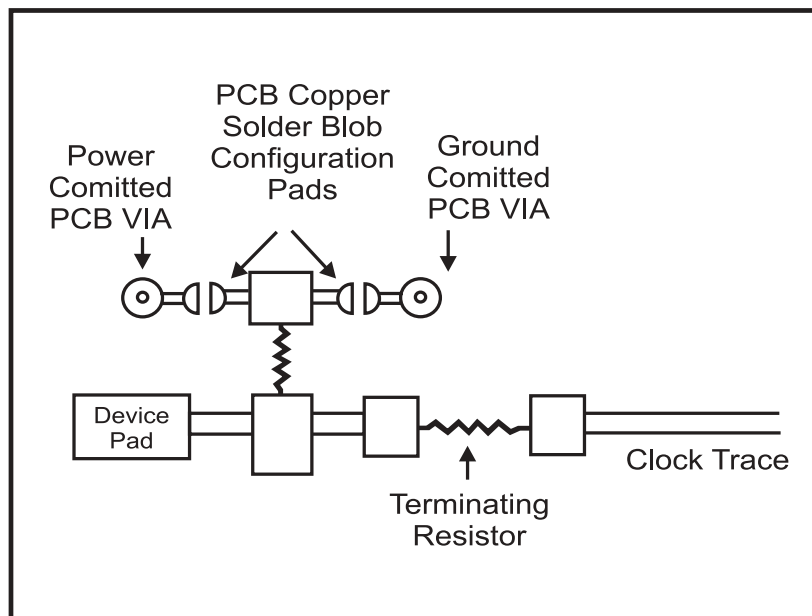


Fig. 2b



Absolute Maximum Ratings

| | |
|-------------------------------|--------------------------------|
| Supply Voltage | 7.0 V |
| Logic Inputs | GND -0.5 V to $V_{DD} + 0.5$ V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Case Temperature | 115°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = V_{DDL} = 3.3$ V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|------------------|--|----------------|--------|----------------|-------|
| Input High Voltage | V_{IH} | | 2 | | $V_{DD} + 0.3$ | V |
| Input Low Voltage | V_{IL} | | $V_{SS} - 0.3$ | | 0.8 | V |
| Input High Current | I_{IH} | $V_{IN} = V_{DD}$ | | 0.1 | 5 | mA |
| Input Low Current | I_{IL1} | $V_{IN} = 0$ V; Inputs with no pull-up resistors | -5 | 2.0 | | mA |
| Input Low Current | I_{IL2} | $V_{IN} = 0$ V; Inputs with pull-up resistors | -200 | -100 | | mA |
| Operating Supply Current | $I_{DD3.3OP}$ | $C_L = 0$ pF; 66.8 MHz | | 100 | 160 | mA |
| Input frequency | F_i | $V_{DD} = 3.3$ V; | | 14.318 | | MHz |
| Input Capacitance ¹ | C_{IN} | Logic Inputs | | | 5 | pF |
| | C_{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T_{trans} | To 1st crossing of target Freq. | | | 2 | ms |
| Settling Time ¹ | T_s | From 1st crossing to 1% target Freq. | | | | ms |
| Clk Stabilization ¹ | T_{STAB} | From $V_{DD} = 3.3$ V to 1% target Freq. | | | 2 | ms |
| Skew ¹ | $T_{CPU-SDRAM1}$ | $V_T = 1.5$ V; SDRAM Leads | -500 | 200 | 500 | ps |
| | $T_{CPU-PCI1}$ | $V_T = 1.5$ V; CPU Leads | 1 | 2.8 | 4 | ns |
| | $T_{CPU-AGP}$ | $V_T = 1.5$ V; CPU Leads | -1 | 0 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3$ V +/-5%, $V_{DDL} = 2.5$ V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|------------------|---|------|-----|-----|-------|
| Operating Supply Current | $I_{DD2.5OP}$ | $C_L = 0$ pF; 66.8 MHz | | 10 | 20 | mA |
| Skew ¹ | $T_{CPU-SDRAM2}$ | $V_T = 1.5$ V; $V_{TL} = 1.25$ V; SDRAM Leads | -500 | 200 | 500 | ps |
| | $T_{CPU-PCI2}$ | $V_T = 1.5$ V; $V_{TL} = 1.25$ V; CPU Leads | 1 | 2.7 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------|---|------|-----|-----|-------|
| Output High Voltage | VOH2B | $I_{OH} = -8 \text{ mA}$ | 2 | 2.2 | | V |
| Output Low Voltage | VOL2B | $I_{OL} = 12 \text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | IOH2B | $V_{OH} = 1.7 \text{ V}$ | | -20 | -16 | mA |
| Output Low Current | IOL2B | $V_{OL} = 0.7 \text{ V}$ | 19 | 26 | | mA |
| Rise Time | tr2B ¹ | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.0 \text{ V}$ | | 1.5 | 1.8 | ns |
| Fall Time | tf2B ¹ | $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1.6 | 1.8 | ns |
| Duty Cycle | dt2B ¹ | $V_T = 1.25 \text{ V}$ | 40 | 47 | 55 | % |
| Skew | tsk2B ¹ | $V_T = 1.25 \text{ V}$ | | 60 | 250 | ps |
| Jitter, Single Edge Displacement ² | tjsed2B ¹ | $V_T = 1.25 \text{ V}$ | | 200 | 250 | ps |
| Jitter, One Sigma | tj1s2B ¹ | $V_T = 1.25 \text{ V}$ | | 65 | 150 | ps |
| Jitter, Absolute | tjabs2B ¹ | $V_T = 1.25 \text{ V}$ | -300 | 160 | 300 | ps |

¹ Guaranteed by design, not 100% tested in production.

² Edge displacement of a period relative to a 10-clock-cycle rolling average period.

Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|----------------------------------|---|------|------|-----|-------|
| Output High Voltage | V_{OH2A} | $I_{OH} = -28 \text{ mA}$ | 2.5 | 2.6 | | V |
| Output Low Voltage | V_{OL2A} | $I_{OL} = 27 \text{ mA}$ | | 0.35 | 0.4 | V |
| Output High Current | I_{OH2A} | $V_{OH} = 2.0 \text{ V}$ | | -29 | -23 | mA |
| Output Low Current | I_{OL2A} | $V_{OL} = 0.8 \text{ V}$ | 33 | 37 | | mA |
| Rise Time | t _{r2A} ¹ | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | | 1.75 | 2 | ns |
| Fall Time | t _{f2A} ¹ | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1.1 | 2 | ns |
| Duty Cycle | d _{t2A} ¹ | $V_T = 1.5 \text{ V}$ | 45 | 50 | 55 | % |
| Skew | t _{sk2A} ¹ | $V_T = 1.5 \text{ V}$ | | 50 | 250 | ps |
| Jitter, One Sigma | t _{j1s2A} ¹ | $V_T = 1.5 \text{ V}$ | | 65 | 150 | ps |
| Jitter, Absolute | t _{jabs2A} ¹ | $V_T = 1.5 \text{ V}$ | -250 | 165 | 250 | ps |

¹ Guaranteed by design, not 100% tested in production.



Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------------|--|------|------|------|-------|
| Output High Voltage | V _{OHI} | I _{OH} = -28 mA | 2.4 | 3 | | V |
| Output Low Voltage | V _{OLl} | I _{OL} = 23 mA | | 0.2 | 0.4 | V |
| Output High Current | I _{OHI} | V _{OH} = 2.0 V | | -60 | -40 | mA |
| Output Low Current | I _{OLl} | V _{OL} = 0.8 V | 41 | 50 | | mA |
| Rise Time ¹ | T _{rl} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 1.75 | 2 | ns |
| Fall Time ¹ | T _{fl} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | | 1.5 | 2 | ns |
| Duty Cycle ¹ | D _{tl} | V _T = 1.5 V | 45 | 50 | 55 | % |
| Skew ¹ | T _{skl} | V _T = 1.5 V | | 200 | 500 | ps |
| Jitter, One Sigma ¹ | T _{j1s1} | V _T = 1.5 V | | 50 | 150 | ps |
| Jitter, Absolute ¹ | T _{jabs1} | V _T = 1.5 V (with synchronous PCI) | -250 | | +250 | ps |
| Jitter, Absolute ¹ | T _{jabs1} | V _T = 1.5 V (with asynchronous PCI) | -400 | | 400 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------------|--|------|-----|-----|-------|
| Output High Voltage | V _{OHI} | I _{OH} = -28 mA | 2.4 | 3 | | V |
| Output Low Voltage | V _{OLl} | I _{OL} = 23 mA | | 0.2 | 0.4 | V |
| Output High Current | I _{OHI} | V _{OH} = 2.0 V | | -60 | -40 | mA |
| Output Low Current | I _{OLl} | V _{OL} = 0.8 V | 41 | 50 | | mA |
| Rise Time | t _{rl} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 1.8 | 2 | ns |
| Fall Time | t _{fl} ¹ | V _{OH} = 2.4 V, V _{OL} = 0.4 V | | 1.6 | 2 | ns |
| Duty Cycle | d _{tl} ¹ | V _T = 1.5 V | 45 | 51 | 55 | % |
| Skew | t _{skl} ¹ | V _T = 1.5 V | | 130 | 250 | ps |
| Jitter, One Sigma ¹ | t _{j1s1a} | V _T = 1.5 V, synchronous | | 40 | 150 | ps |
| | t _{j1s1b} | V _T = 1.5 V, asynchronous | | 200 | 250 | ps |
| Jitter, Absolute ¹ | t _{jabs1a} | V _T = 1.5 V, synchronous | -250 | 135 | 250 | ps |
| | t _{jabs1b} | V _T = 1.5 V, asynchronous | -650 | 500 | 650 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - AGP

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$; $C_L = 30 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------|--|-----|-----|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -28 \text{ mA}$ | 2.4 | 3 | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 23 \text{ mA}$ | | 0.2 | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0 \text{ V}$ | | -60 | -40 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8 \text{ V}$ | 41 | 50 | | mA |
| Rise Time | t_{r1}^1 | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | | 1.1 | 2 | ns |
| Fall Time | t_{f1}^1 | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | | 1 | 2 | ns |
| Duty Cycle | d_{t1}^1 | $V_T = 1.4 \text{ V}$ | 45 | 49 | 55 | % |
| Skew | t_{sk1}^1 | $V_T = 1.5 \text{ V}$ | | 130 | 250 | ps |
| Jitter, One Sigma ¹ | t_{j1s1} | $V_T = 1.5 \text{ V}$ | | 2 | 3 | % |
| Jitter, Absolute ¹ | t_{abs1a} | $V_T = 1.5 \text{ V}$, synchronous | -5 | 2.5 | 5 | % |
| | t_{abs1b} | $V_T = 1.5 \text{ V}$, asynchronous | -6 | 4.5 | 6 | % |

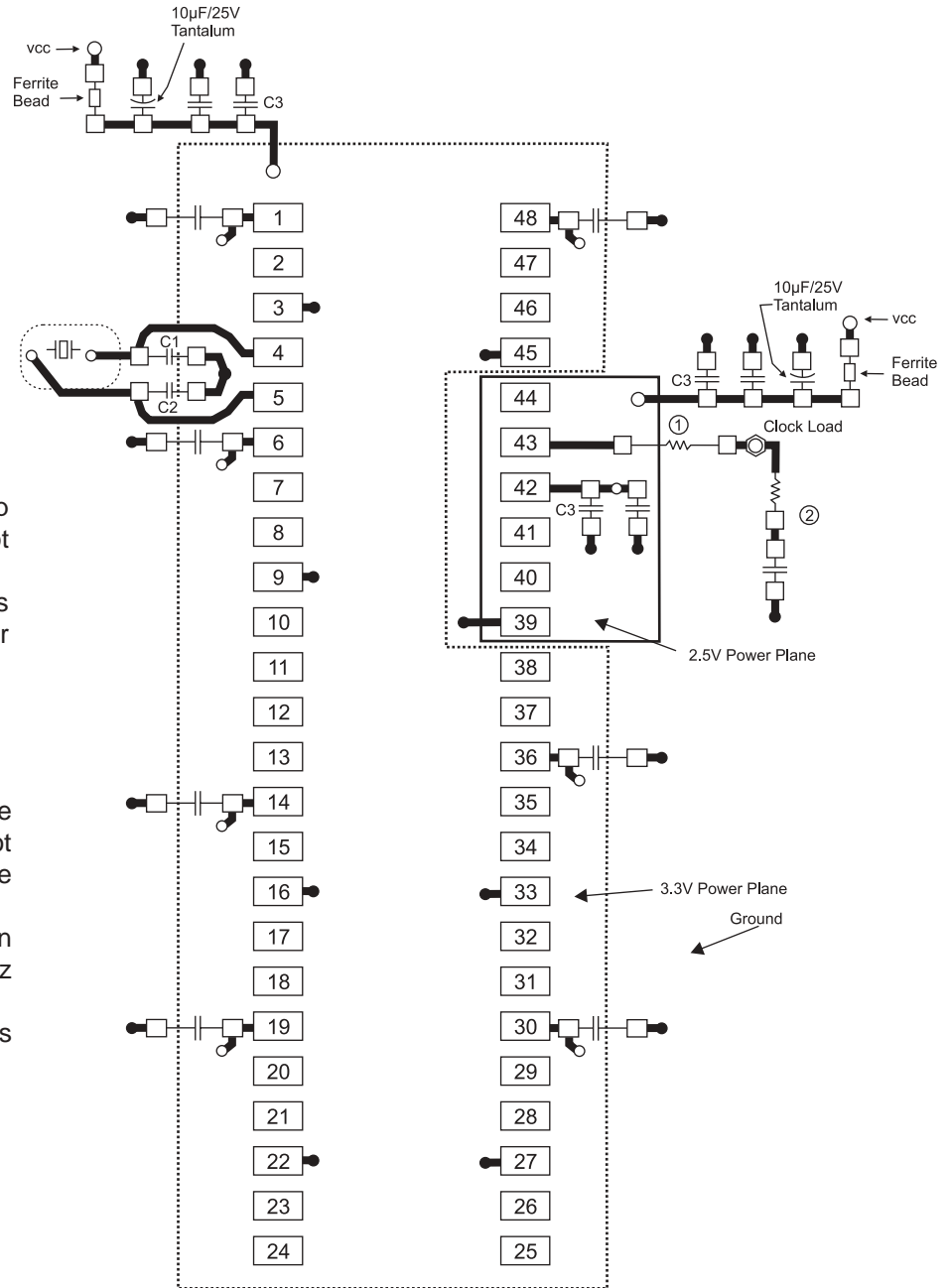
¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz, REF0

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|---------------|--|-----|-----|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -16 \text{ mA}$ | 2.4 | 2.6 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9 \text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0 \text{ V}$ | | -32 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8 \text{ V}$ | 16 | 25 | | mA |
| Rise Time | t_{r5}^1 | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | | 2 | 4 | ns |
| Fall Time | t_{f5}^1 | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | | 1.9 | 4 | ns |
| Duty Cycle | d_{t5}^1 | $V_T = 1.5 \text{ V}$ | 45 | 54 | 57 | % |
| Jitter, One Sigma | t_{j1s5}^1 | $V_T = 1.5 \text{ V}$ | | 1 | 3 | % |
| Jitter, Absolute | t_{jabs5}^1 | $V_T = 1.5 \text{ V}$ | -5 | - | 5 | % |

¹Guaranteed by design, not 100% tested in production.



General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

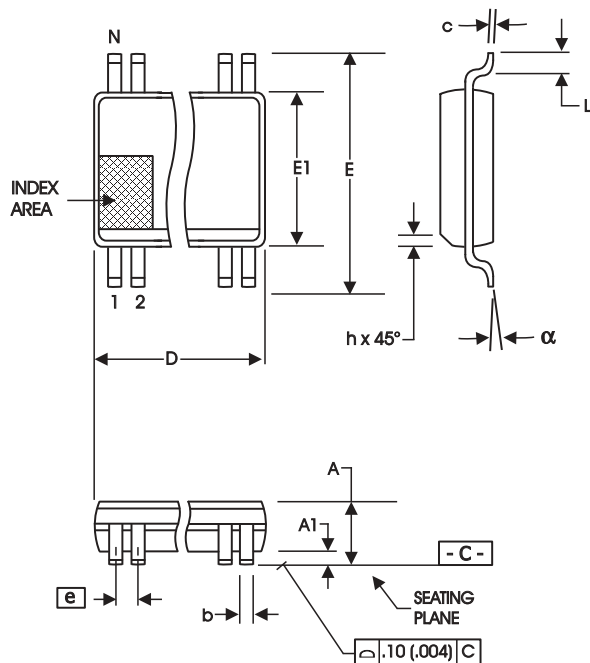
Notes:

- 1) All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram.
- 2) 47 ohm / 56pf RC termination should be used on all over 50MHz outputs.
- 3) Optional crystal load capacitors are recommended.

Connections to VDD:

- Best
- Okay
- Avoid
- Avoid

- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads
- ⊗ = Clock Load



300 mil SSOP

| SYMBOL | In Millimeters | | In Inches | |
|--------|-------------------|-------|-------------------|-------|
| | COMMON DIMENSIONS | | COMMON DIMENSIONS | |
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9148yF-37 LF-T

Example:

ICS XXXX y F PPP LF-T

