Headland
Technology Inc

HT21
PC/AT Compatible Single Chip

T-52-33-01

FEATURES

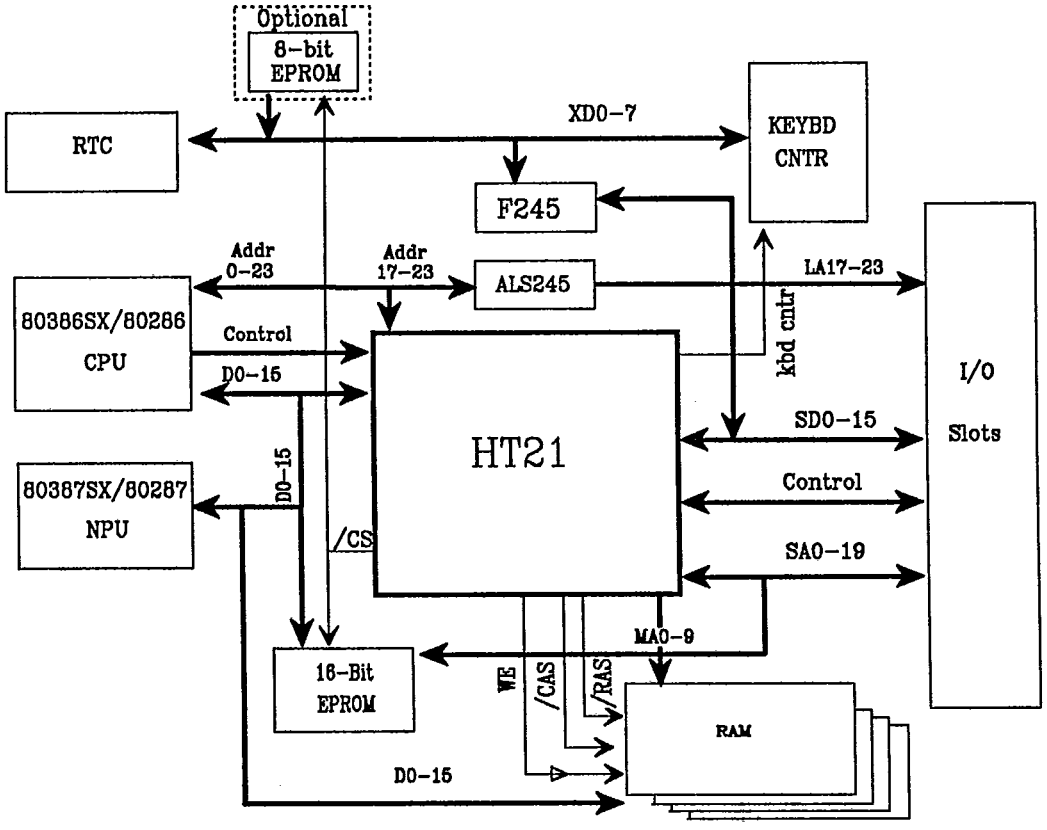
- **Single Chip 80386SX/80286 PC/AT Compatible Solution for CPU Clock Speeds to 16MHz SX Mode or 20MHz 286 Mode**
- **Supports up to 8 MB DRAM using 1M or 256K Devices**
- **Page Mode and 2 or 4-Way Interleaving**
- **LIM EMS 4.0 Support in Hardware using 2 Sets of 32 EMS Registers**
- **8 Bit or 16 Bit BIOS Support**
- **Asynchronous AT Bus Clock**
- **Supports up to 12 MHz Backplane Operation**
- **Programmable DRAM Timing**
- **Pin Compatible with Future Single Chips**
- **Fast A20GATE and Hot Reset**
- **Pipeline Mode Operation**
- **HCMOS Technology**

DESCRIPTION

The HT21 is an advanced PC/AT compatible high integration, single chip 80386SX/80286 solution. This highly integrated single-chip solution features high performance, low power consumption, extremely low board-space requirements, advanced memory management features which include support for page mode and 2 or 4-way interleaving. The EMS 4.0 hardware implementation with dual sets of 32 registers and full context support has been optimized for the highest performance local memory accesses. A complete PC/AT compatible system may be implemented with minimal external support logic. Advanced EMS hardware write-protect has been added for maximum EMS 4.0 compatibility. Supports 256K and 1M DRAMs in configurations up to 8MB of on-board system memory as well as Shadow RAM for System and Video BIOS at zero or one wait state.

The HT21 performs CPU and peripheral support functions including that of DMA Controllers, a Memory Mapper, Timers, Counters, Interrupt Controllers, a Bus Controller and their supporting circuitry. This chip also includes address buffers, data transceivers, memory drivers, parity checking and supporting circuitry. An asynchronous AT Bus clock allows for a constant 8MHz Bus clock rate. This device is packaged in a 208 pin Plastic Quad Flat Pack.

System Board Block Diagram



The HT21 single chip, integrates the control logic and peripheral logic of the 80386SX/80286 AT architecture and provides the necessary control to buffer the addresses of the A, SA, and MA buses. Peripheral circuits embedded in this device include: an 82284, 74612, 8284, 8254, two 8237s, and two 8259s. The 82284 generates PROCCLK, /READY and /RESET for system use. It also provides all the CPU I/O command signals for memory, peripherals, and add-on boards. The EMS Auto-Increment provides the capability to emulate multiple contexts for use with advanced multi-tasking requirements. A 9-bit refresh counter produces the row address of memory during refreshes. The 74612 supplies memory mapping addresses. An 8284 uses the 14.318 MHz input clock to generate OSC and a base clock for the 8254 timer/counter. This timer is programmed by the CPU and provides signals for system timing, refresh, and speaker tone generation. The CPUHLDA signal controls the Address bus (A) flow between the CPU and the Slot expansion (SA) bus. The Memory Address (MA) bus is generated by multiplexing the expansion (SA) bus.

On power up the EMS function is disabled, all the DRAM addresses are left as flat linear addresses; ie. without any EMS translations. An internal Linear Address Decoder accesses the lower 0-640K and 1 Meg and above -- to the upper limit of the system's memory. Bank selection can be controlled in software; where bits D5 and D6 of the Map Register (1EC) determine the number of banks.

Another I/O register selects the EMS pages; with the (address space from 256K(40000) to 640K(A0000) and from768K(C0000) to 896K(DFFFF) being decoded as 32 pages. To get 64K of program memory, four contiguous pages are required. The EMS pages are accessed through the Map Address Register located at I/O address 1EE(hex); which is a read/write register.

The hardware has been optimized to allow mixing of 256K and 1M DRAM in different banks to give maximum flexibility and support for multiple Shadow RAM address relocation, Interleave and refresh. When the split feature is active all memory is relocated upward by 384K. Two 8259s are configured as master/slave; they receive interrupt requests from a timer, keyboard controller, a real time clock, the numeric processor and up to 11 other sources. They issue a signal to the CPU to initiate interrupt routines. The HT21 converts 16-bit buses for peripherals having only 8-bit wide buses; thus maintaining compatibility with the 8088 PC. The HT21 also has parity checking logic for board implementations that require parity checking.

An asynchronous AT Bus Clock can be implemented allowing the AT Bus to operate at a frequency, different than the main memory. This feature will allow the AT Bus to operate at a constant 8MHz if so desired.

OS/2 Optimization

OS/2 Optimization consists of two specific enhancements to the original AT design. These are the Alternate Gate A20 (Bit 1 of the Port 92H) and Alternate Hot Reset (Bit 0 of the Port 92H) features.

The Alternate Gate A20 feature is used to force address A20 to low (inactive) whenever the processor is in Real Address Mode. (This is required to insure 8086 compatibility). The CPU Reset feature is used to change the CPU from Virtual Address Mode back to Real Address Mode. A CPU reset is the only way to make this mode change.

In the original AT both of these functions were handled through the keyboard controller. The keyboard controller, however, is a very slow device. Therefore, in order to improve the performance of these features, the HT21 implements parallel circuitry that performs the same functions at a much faster speed. The new circuitry is implemented in parallel and the old circuitry is retained to ensure full AT compatibility. These enhancements are referred to as OS/2 Optimization because these features are used by OS/2 which gains performance from the enhancement.

Alternate Gate A20 is a read/write bit controlling address bit A20 when CPU is in the Real Address Mode.

1 = A20 is active
0 = A20 is inactive

This bit is set to 0 during system reset.

Alternate Hot Reset is also a read/write bit providing an alternate CPU reset function, which supports faster operation than the original implementation on the standard AT using the 8042 controller for a mode switch from the Protected Virtual Address Mode to the Real Address Mode.

This Alternate Hot Reset is used to increase system performance when switching from protected to real mode. This bit must be set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, this Alternate Hot Reset pin is pulsed high for 100 to 125 ns, the reset takes place after a minimum delay of 6.72 microseconds. After writing this bit from 0 to 1 the latch remains set to 1.

1 = Assumes a switch from the Protected Mode to Real Mode has taken place.
0 = Assumes the system was just powered on.

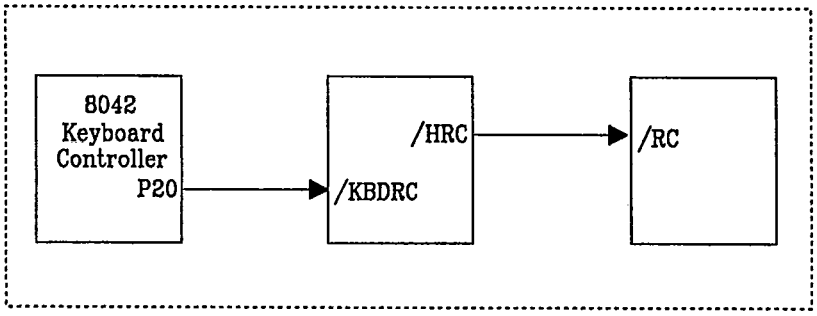
Pipeline Option

The 80386SX processor provides the option of choosing between two types of bus cycle timing, pipeline and non-pipeline. This pipelining option is controlled on a cycle-by-cycle basis with the processors /NA input signal. The two cycle types function as follows.

When non-pipeline timing is selected, the processor will issue address and bus cycle definition signals at the beginning of the first bus state of each bus cycle. The processor will maintain the validity of these signals until it receives an acknowledgement on its /READY input, which terminates the cycle.

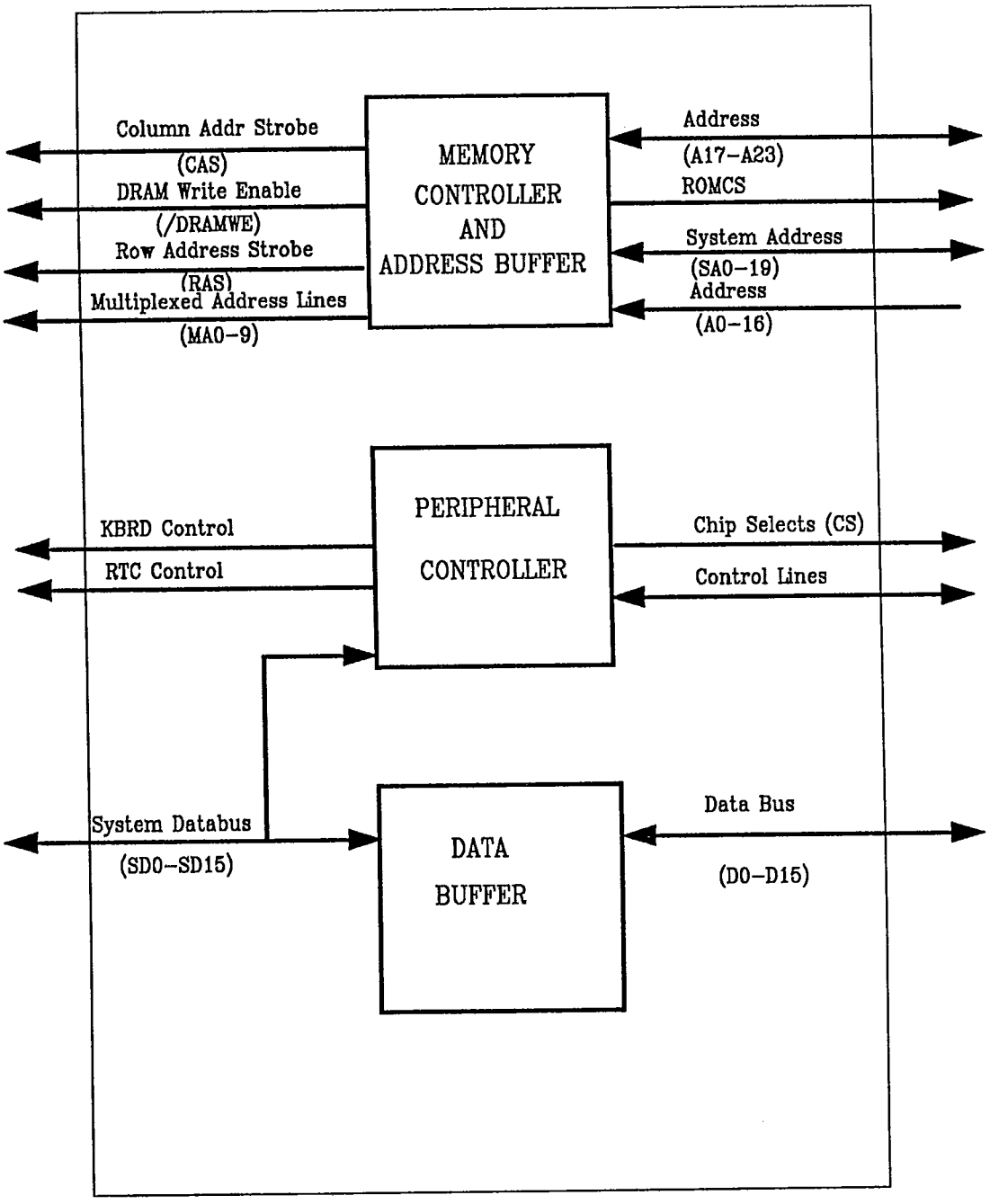
In contrast, when pipelining is selected, the processor outputs the address and bus cycle definition of the next bus cycle (if it is available) without waiting for the current cycle to be acknowledged. This can be advantageous in that the fastest bus cycle with pipelining is the same as without (two bus states), which maintains the same data band width, yet with pipelining the address-to-data access time is increased by one bus state. This in turn eases system timing requirements, such as allowing the use of slower DRAM at the same processor speed.

The only minor drawback to pipelining is that even if it is perpetually selected the processor still requires occasional non-pipeline cycles. Specifically, after any idle bus state, the processor always uses non-pipeline address timing, and then switches to pipeline thereafter. This is due to the fact that the processor initially needs one bus state to "get ahead" of the oncoming bus cycles.

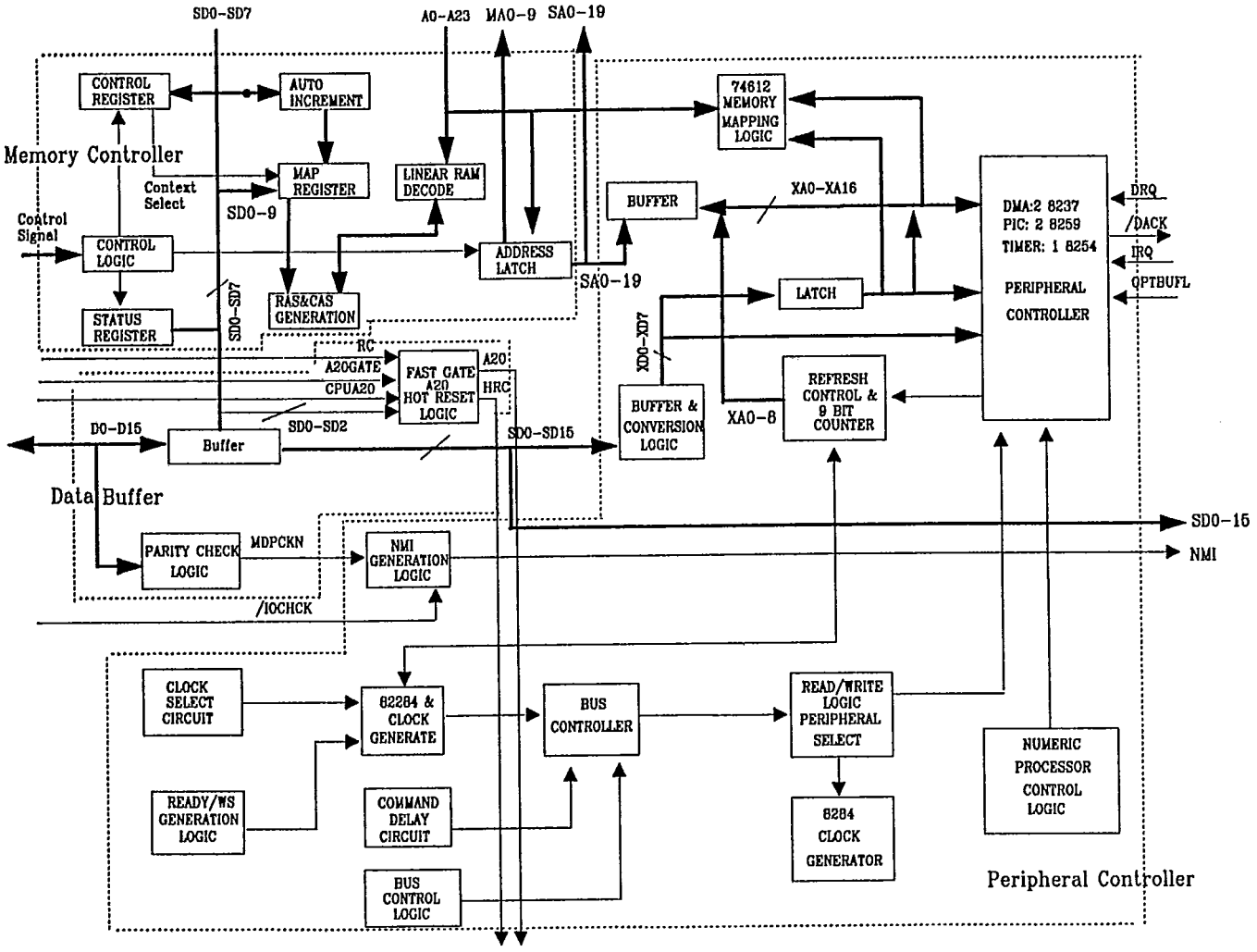


OS/2 OPTIMAZATION

HT21
Chip Block Diagram



HT21
Chip Block Diagram



Clock Switching Logic

The clock switching circuit in the HT21 allows the system PROCCLK to run at two different system speeds. The two clock inputs (CLKX2 and CLKASN) can be connected to two different clock sources. CLKASN is always used for I/O cycles and when low speed is selected for accessing the AT expansion slots. The CLKX2 input will be used when on-board memory is being accessed to get the highest performance possible.

	HISPEED=1 IOSPDIN=0	HISPEED=0 IOSPDIN= Don't Care	HISPEED=1 IOSPDIN=1 *
Clock Source	CLKASN CLKX2	CLKASN CLKX2	CLKASN CLKX2
I/O	X	X	X
Local Memory	X	X	X
AT Bus Access	X	X	X
AT Sysclk (Ext)	X	X	X

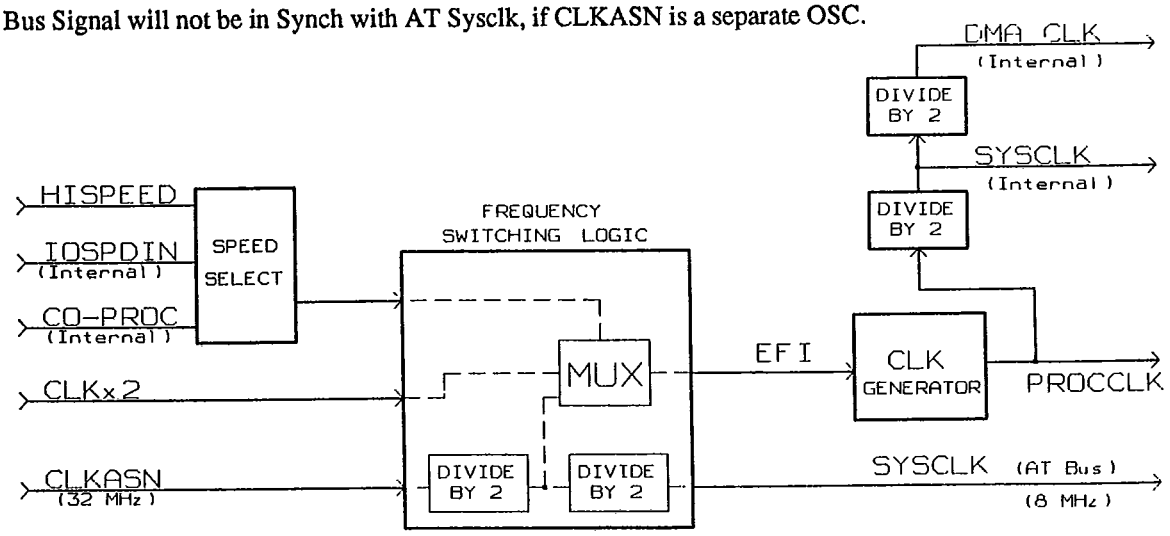
CLKASN input is usually 32 MHz which is divided by two by the HT21 to obtain a frequency of 16 MHz for 8MHz system operating speed. The AT bus SYSCLK is derived from this clock source and hence runs at a constant 8MHz. The frequency of CLKX2 is the desired high speed frequency for the system, ie. 24MHz for a 12MHz system. A system running at 16 MHz, does not require two oscillators for CLKASN and CLKX2. These two inputs can be connected together and fed by a 32MHz oscillator.

The speed selection logic decides at what speed the system should be running by sampling the HISPEED input, the I/O speed input and the internal numeric processor chip select input.

The Frequency switching logic switches between the two clock sources selected by the speed selection logic. For high speed to low speed clock switching, the frequency switching logic will wait until AT bus SYSCLK is at the right phase before it switches over to obtain synchronization between AT Bus SYSCLK and the other control signals (MEMR etc.) on the AT bus. When switching from low speed to high speed, the logic changes at the next correct phase of CLKX2 and AT Bus phase SYSCLK is not considered.

The output of the frequency switching logic is then used internally for generating the internal SYSCLK, DMA clock and clock generator.

* AT Bus Signal will not be in Synch with AT Sysclk, if CLKASN is a separate OSC.



COMMAND DELAY, WAIT STATES BASED ON CYCLE TYPE

	LOCAL ROM READ	LOCAL RAM READ	LOCAL RAM WRITE
COMMAND DELAY	NO	NO	NO

	AT BUS MEMORY 8 BIT	AT BUS MEMORY 16 BIT	AT BUS I/O 8 BIT	AT BUS I/O 16 BIT	AT BUS INTERRUPT ACKNOWLEDGE
COMMAND DELAY	YES	NO	YES	YES	YES
WAIT STATES	4	1	4	1	-

Interleave

Interleave is enabled when an even number of Banks are installed and the DRAM Bank pairs are of the same type. If bit 1 of control register 4 is set to 0 (default), word interleave will be selected. Page interleave will be selected if bit 1 is set to 1.

Refresh

A refresh cycle starts by performing a RAS precharge cycle for all banks of RAM. This is followed by staggered RAS-only refresh cycles. The page registers are reset. The first memory cycle to any bank following a refresh is always a page miss.

DMA or Bus Master

The RAS and CAS timing for the DRAM are generated from the delay lines and the page sequencers are reset. The first memory cycle to any bank following a DMA or Bus Master cycle is a page miss.

HT21
DRAM Settings

REGISTER VALUE				TYPES OF DRAMS INSTALLED					TOTAL
CR0	CR1	CR0		BANK1	BANK2	BANK3	BANK4	Interleave	MB
D7	D6	D6	D5						
Off	Off	Off	Off	256K	None	None	None	0	512K
Off	Off	Off	On	256K	256K	None	None	2	1M
Off	Off	On	Off	256K	256K	256K	None	0	1.5M
Off	Off	On	On	256K	256K	256K	256K	4	2M
Off	On	Off	Off*	256K	64K	None	None	0	640K
Off	On	Off	On	256K	256K	None	None	2	1M
Off	On	On	Off	256K	256K	1M	None	0	3M
Off	On	On	On	256K	256K	1M	1M	2	5M
On	Off	Off	Off	1M	None	None	None	0	2M
On	Off	Off	On	1M	1M	None	None	2	4M
On	Off	On	Off	1M	1M	1M	None	0	6M
On	Off	On	On	1M	1M	1M	1M	4	8M
On	On	Off	Off	1M	None	None	None	0	2M
On	On	Off	On	1M	1M	None	None	2	4M
On	On	On	Off	1M	1M	256K	None	0	4.5M
On	On	On	On	1M	1M	256K	256K	2	5M

* SPLSW must be On.

On - pin grounded

Off - pin not grounded

I/O Address Map

Hex Range	Device Address	Part Number
000 - 0FF	Reserved for System board I/O	
000 - 01F	DMA Controller #1	8237A-5
020 - 03F	Interrupt Controller #1	8259A
040 - 05F	Timer	8254-2
060,062 - 06F	Keyboard Controller	8042
061	Port B Register,PPI	8255
070 - 07F	Real Time Clock, NMI (Non-interruptable Mask) bit	
080 - 08F	DMA Page Register	74LS612
090 - 091	DMA Map Register	
092	Alternate Gate A20 and Hot Reset	
093 - 09F	DMA Map Register	
0A0 - 0BF	Interrupt Controller #2	8259A
0C0 - 0DF	DMA Controller #2	8237A-5
0F0	Clear Math Coprocessor Busy	
0F1	Reset Math Coprocessor	
0F8 - 0FF	Math Coprocessor	80287 only
1EC-1EF	EMS and Control Registers	

PORT B (8255) PPI Register, Address 61h

Data Written		
	Bit 3 = 1	Disable NMI for IOCHCK(*)
	Bit 2 = 1	Disable NMI for Memory Parity error
	Bit 1	Speaker data
	Bit 0 = 1	Enable Timer (8254) for speaker
Data read back		
	Bit 7 = 1	Memory Parity error
	Bit 6 = 1	IOCHCK error(*)
	Bit 5	Timer 2 (8254), output
	Bit 4	REFRESH detect
	Bit 3 = 1	NMI disabled, for IOCHCK(*)
	Bit 2 = 1	NMI disabled for Memory Parity error(*)
	Bit 1	Speaker data
	Bit 0 = 1	Timer 2 (8254) for speaker enabled

EMS Register Summary

The HT21 contains three internal EMS Read/Write registers, all accessed via I/O operations. They are the Map Address Register (MAR) at 1EE, the Control Register (CR) at 1EF, and the Map Register (MR) at 1EC. The first two registers are 8 bits wide (I/O byte operations); the Map Register is 10 bits wide and thus requires I/O word accesses.

During I/O cycles, the Map Address Register(1EE) provides a 6-bit address to the Map Register (a 64x10 Static RAM). This selects the register for programming or reading the maps. Writing data to the Map Register(1EC) programs the RAM, and that data becomes the uppermost address bits (translated A14-A19) when addressing DRAM in EMS operation. By selecting the auto-increment operation of the Map Address Register, you can write once to the Map Address Register, and follow that with 64 writes to the Map Register and fully program the RAM pages with the address translations. This programs both the standard and alternate context maps.

During memory cycles, address pins and a single bit from the Control Register(1EF) provide the 6-bit address to the Map Register(1EC). The Map Register then puts its programmed data onto the system's external DRAM address lines.

The Map Register contains two sets of 32 registers; used as standard context maps and alternate context maps. This allows two programs to maintain separate and simultaneous register mappings, so switching between two programs is practically instantaneous. In systems with only a single set of 32 registers, when a second program needs to perform EMS operations, it must save the current mapping and then write it's own maps before starting. This requires time, and data may be lost in fast-moving communications programs. The two sets of 32 registers in the HT21 alleviate this problem.

For I/O cycles, the Map Address Register(1EE) page bits (D0-D4) select 1 of 32 registers, and its Context bit (D5) selects between the two pairs of 32 registers. 0 selects the standard context maps, and 1 selects the alternate context maps. These six bits drive the address lines of the 64x10 RAM, or Map Register. An additional bit determines whether auto-incrementing is enabled (D7). If enabled, when a count of all ones is reached on D0-D6, D7 is cleared and auto-incrementing ceases.

For the memory cycles, 6 address pins select pages among the 32 registers. The address pins are either A14-A19 or SA14-SA19, depending upon whether the CPU has control of the system or not. Multiplexing of the 3 upper addresses, ie A17-A19, reduces this 6-bit address to 5 inputs to the Map Register. As with I/O cycles, there is a Context bit to select between the 2 sets of 32 registers. D0 of the Control Register(1EF) provides context information; a 0 selects the standard context maps.

The Map Register outputs 10 lines, the 7 least significant provide DRAM addresses, the next two perform bank selection and thus generate RAS0-RAS3, and D9 is for bank enable. When EMS memory accesses occur, A0 to A13 are passed unfiltered to the DRAM. A14 to A19 are redirected to the MR as addresses, and the Map Register outputs the translated addresses on its D0-D6 lines. (The smaller 256K DRAM uses only D0-D4 outputs.)

Four other bits within the Control Register, D7-D5 and D2, are software switches to select DRAM type (1M vs 256k DRAM), bank count, and extra 384K disable . The same functions can be controlled by grounding four pins on the HT21, respectively: RAM1M, RAMSW2 and RAMSW1 and SPLSW.

The full EMS register descriptions follow.

Page Size Description

Page Size

4 Way Interleave

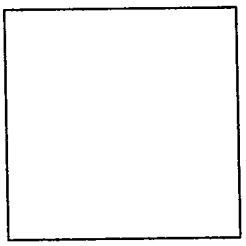
256K	256K	256K	256K	Device Type
4 X 1024 Bytes				
4096 Bytes				

1Meg	1Meg	1Meg	1Meg	Device Type
4 X 2048 Bytes				
8192 Bytes				

TYPICAL
DRAM
ORGANIZATION

CAS 1024

RAS
1024

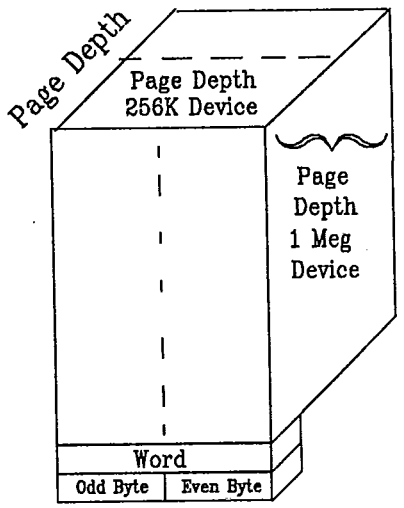


1 Meg DRAM

Page Size

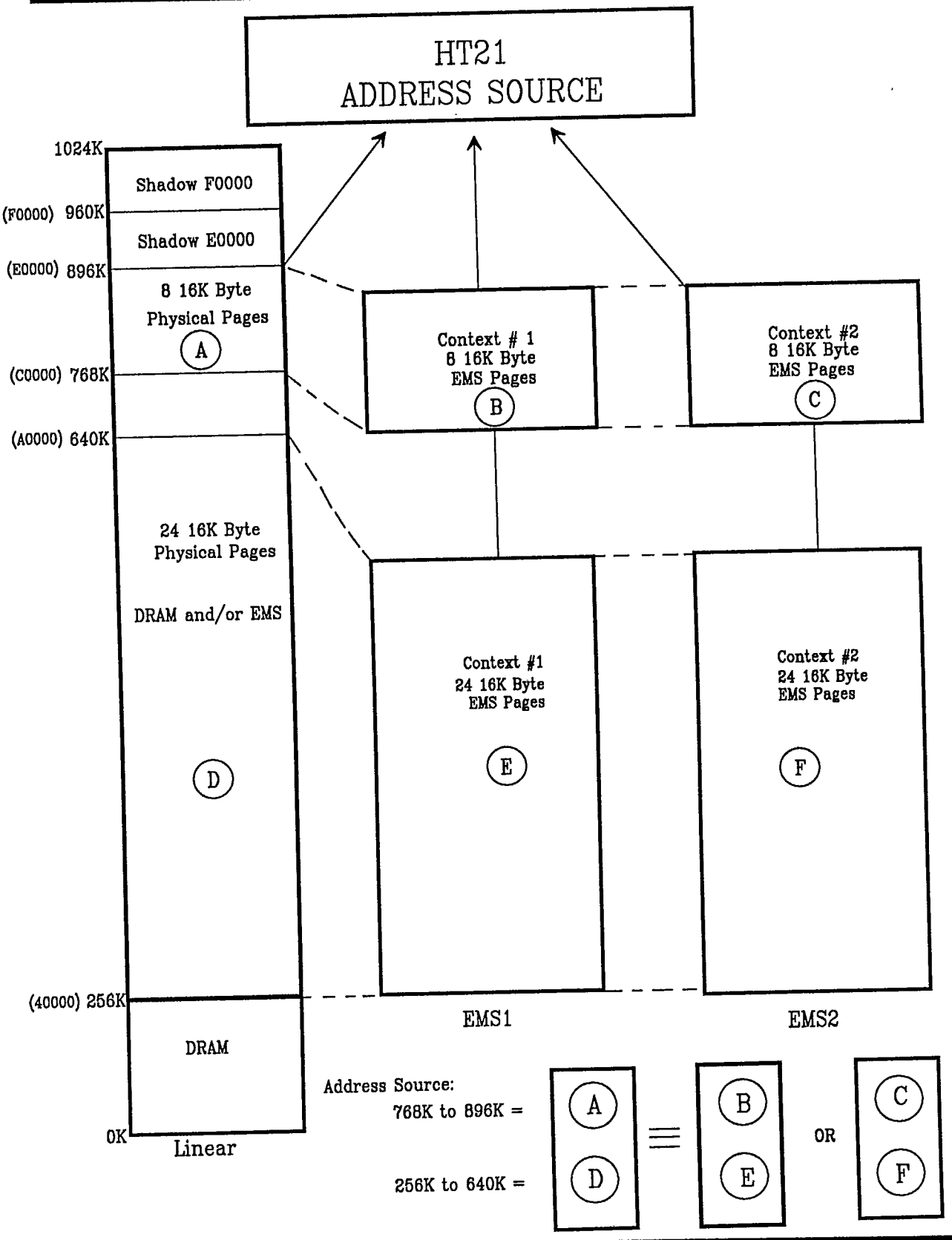
1024 X 16 Bits
= 1024 Word's
= 2048 Bytes

PAGE
DESCRIPTION



256K DRAM

HT21
Memory Map



MAP ADDRESS REGISTER 8R/W bits at I/O address 1EE (hex) Reset State:0	
D7	Auto-increment Enable Bit
D6	EMS Page Write Protect
D5	Context Selection
D4-D0	Page Selection 1 page (or more) of 32

D7: Auto-increment, Enable

When 1, each read or write of the Map Register (1EC) increments the count on D7-D0. These bits can be treated as a 8-bit counter, which auto-increments under D7 control. The counter consists of Auto-increment Enable (D7), EMS Page Write Protect (D6), Context Selection (D5), and Page Address bit (D4-D0).

By initializing the counter to 80 hex (auto-incrementing on, standard context, and page 40,000 hex) the maximum number of automatic accesses is available. 32 standard-context writes are followed by 32 alternate-context writes; bringing the count to C0. Then, 32 reads in each context would increment the counter to 00. The 64th read clears the auto-incrementing enable (D7), and prevents further increments until D7 is manually set back to 1.

D6: EMS Page Write Protect

With D6 = 0, Do not write protect the selected page when data is written to the Map Register to select the physical memory to map into this EMS page.

With D6 = 1, Write protect the selected page when data is written to the map register to select the physical memory to map.

D5: Context Selection

When 0, standard context is the default
When 1, alternate context

The HT21 contains two sets of 32 registers, each maps to different available pages. Bit D5 switches between the two sets of registers during I/O cycles. (CR's D0 is context selection during memory cycles.) This allows one program to access its 32 mapping registers (standard context), and a second program has an alternate set of register maps (alternate context). With two pairs of registers available, changing between two programs is almost instantaneous, and data integrity is maintained. D5 selects the active set of map registers during I/O EMS cycles.

D4-D0: Page Selection

D4-D0: Page Selection

Page selection is determined by these 5 bits. Once latched in the MAR, with incrementing enabled, they generate the address lines to the Map Register for I/O cycles. Select the appropriate page(s) by setting D4-D0 according to Table 1 below. A minimum of 4 contiguous 16k pages must be selected for EMS operation. (EMS requires a Page Frame size of 64K or more, thus four 16K pages.) Note that page addresses are presented in the table below as both hexadecimal and decimal numbers.

Hexadecimal Page Address	Decimal Page Address	Register 1EE Bits D 4	DDDD 3 2 1 0
DC000-DFFFF	880-896K	1	1111
D8000 -	864 -	1	1110
D4000 -	848 -	1	1101
D0000 -	832 -	1	1100
CC000-CFFFF	816 - 832K	1	1011
C8000 -	800 -	1	1010
C4000 -	784 -	1	1001
C0000-C3FFF	768 - 784K	1	1000
....	... ...	....	
9C000-9FFFF	624 - 640K	1	0111
98000 -	608 -	1	0110
94000 -	592 -	1	0101
90000 -	576 -	1	0100
8C000-8FFFF	560 - 576K	1	0011
88000 -	544 -	1	0010
84000 -	528 -	1	0001
80000 -	512 -	1	0000
7C000-7FFFF	496 - 512K	0	1111
78000 -	480 -	0	1110
74000 -	464 -	0	1101
70000 -	448 -	0	1100
6C000-6FFFF	432 - 448K	0	1011
68000 -	416 -	0	1010
64000 -	400 -	0	1001
60000 -	384 -	0	1000
5C000-5FFFF	368 - 384K	0	0111
58000 -	352 -	0	0110
54000 -	336 -	0	0101
50000 -	320 -	0	0100
4C000-4FFFF	304 - 320K	0	0011
48000 -	288 -	0	0010
44000 -	272 -	0	0001
40000-43FFF	256 - 272K	0	0000
(4000 increments hex	16k increments) decimal		

MAP REGISTER 10 R/W bits, at I/O address 1EC (hex) Reset State: 0	
D9	Map Enable
D8-D7	Bank Select
D6-D5	1M DRAM Address Bits
D4-D0	1M/256K DRAM Address Bits

D9 Map Enable

When the Global EMS Enable bit in Control Register 0 is a 1, the Map Enable bit associated with each 16K page acts as an individual page mapping enable. If Map Enable is a 1, then its corresponding page is remapped by the HT21. If the Map Enable bit is 0, the CPU address lines are passed through untranslated. If the Global EMS Enable bit is a 0, all address remapping is turned off regardless of the state of the individual Map Enable bits.

D8-D7 Bank Select For 1M/256k, selection as follows:

D8	D7	
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

D6-D5 Translated address bits for 1 Meg DRAMS They drive A20 and A19 (A18-A14 see below) on system DRAMs.

D4-D0 Translated address bits for 256K/1M DRAMs They drive A18 to A14 on system DRAMs.

CONTROL REGISTER INDEX 8R/W bits, at I/O 1ED (hex) Reset State: 0	
D7-D3	Reserved
D2-D0	Control Register Select at 1EF (Hex)

D7-D3: Reserved: Write as zero

D2-D0 Control Register Select:

D2	D1	D0	
0	0	0	Control Register 0
0	0	1	Control Register 1
0	1	0	Control Register 2
0	1	1	Control Register 3
1	0	0	Control Register 4

CONTROL REGISTER 0 8 R/W bits, at I/O address 1EF (hex) Reset State: all 0's	
D7	DRAM-type
D6-D5	DRAM Bank-count
D4	Shadow Enable, F0000 and FF0000
D3	Shadow Enable, E0000 and FE0000
D2	Extra 384k Disable
D1	Global EMS Enable
D0	Context Selection

D7 DRAM Type

1 = 1M DRAMs
0 = 256K DRAMs (default)

D6-D5 DRAM Bank-count

This register is used to program the number of banks installed under BIOS control.

D6	D5	RAM Banks Enabled	Interleave Mode
0	0	1	0
0	1	2	2
1	0	3	0
1	1	4	4

D4 Shadow Enable F0000 (source) and FF0000 (shadow)

64K page of DRAM that would have been located from F0000 to FFFFF is now enabled between 0F0000 to 0FFFFF and is duplicated at FF0000 to FFFFFF. The ROM chip select will now be disabled. Data should be written to this DRAM before enabling this bit. Access to this memory requires the following EMS pages be reserved for shadow ram use:

256KDRAMS Installed		1M DRAMs Installed	
High	/Low Byte	High	/Low Byte
02	9C	02	3C
02	9D	02	3D
02	9E	02	3E
02	9F	02	3F

Note: DRAM is write protected in these Ranges and is READ only.

D3 Shadow Enable E0000 (source) and FE0000 (shadow)

The 64K page of DRAM that would have been located from E0000 to EFFFF is now enabled between 0E0000 and 0EFFFF and is duplicated at FE0000 to FEFFFF. The ROM chip select will now be disabled. Data should be written to this DRAM before enabling this bit. Access to this memory requires the following EMS pages be reserved for shadow DRAM use:

256K DRAMs Installed		1M DRAMs Installed	
High	/Low Byte	High	/LowByte
02	98	02	38
02	99	02	39
02	9A	02	3A
02	9B	02	3B

Note: DRAM is write protected in this Range and is READ only.

D2 Extra 384K Disable

This register bit disables/enables the 384K. A 1 written to D2 disables the extra 384K, a 0 enables it.

Normally the 384K address range, located between A0000 and 1 Meg, is relocated above the 1M border. This preserves the lower addresses for system use. D2=1, the relocated 384K is disabled and usable as shadow RAM or as EMS.

D1 Global EMS Enable

If D1 = 1, EMS memory is enabled. You must initialize the EMS registers before D1 is set high.

D0 Context Selection

If D0 = 0, the standard context is selected; if 1, the alternate context. This bit operates in the same manner as bit D5 of Register 1EE, except this determination of context is used during Memory cycles.

CONTROL REGISTER 1 8 R/W bits at I/O address 1EF (Hex) Reset State: 0	
D7	Page Mode Enable
D6	Mix Dram Type
D5-D3	RAS Precharge timing
D2-D0	RAS Active Timeout

D7: Page Mode Enable
0 Page mode disabled, uses delay line timing for normal memory access
1 Page mode enabled, uses synchronous memory timing except during DMA and bus master

D6: Mix Dram Type Mode Register

D6	Memory Type
0	Same type all four banks
1	Selected type first 2 banks, other type last two banks
	Special CASE when 256K DRAMs, selected and only 1 bank is selected the use of 256K DRAMs in the first bank and 64K DRAMs in the second bank is allowed for a total of 640K RAM. Extra 384K must be disabled.

D5-D3: RAS Precharge Timing

D5	D4	D3	PROCCLK Cycles
0	0	0	16
0	0	1	14
0	1	0	12
0	1	1	10
1	0	0	8
1	0	1	6
1	1	0	4
1	1	1	2

D2-D0: RAS Active Timeout

D2	D1	D0	PROCCLK Cycles
0	0	0	1080
0	0	1	960
0	1	0	840
0	1	1	720
1	0	0	600
1	0	1	480
1	1	0	360
1	1	1	240

Values can be adjusted to provide nominal values near 10 usec for any speed system configuration. A speed timing routine or preset system speeds are required to determine the correct value. All timing is based on a fixed PROCCLK signal. If changes are made to PROCCLK, then register value changes may be required to compensate.

CONTROL REGISTER 2 8 R/W bits, at I/O address 1EF (Hex) Reset State: 0	
D7-D6	Reserved
D5-D4	Page Mode
D3-D2	CAS Precharge Time
D1-D0	CAS Active Time

Values are adjustable to provide values for most all DRAMs at any speed and configuration. All timing is based on a fixed PROCCLK signal. If changes are made to the PROCCLK signal, adjustments may be required to this register to compensate. DD Hex is the recommended value for 80386SX or 80286 0-wait state operation. C8 Hex should be used for 1-wait state 386SX systems while CC Hex should be used for 1-wait state 286 systems.

D7-D6: Reserved

These 2 Bits must be set to 1 in order to execute operations properly.

D5-D4: Page Mode

D5	Non-page Mode Zero Wait State enable Valid when D7 of Control Register 1 is set to 0
0	1 Wait State Memory Operation
1	Assert Zero Wait State all Non-page Mode Memory Cycles
D4	Page Mode Zero Wait State enable Valid when Control Register 1 is set to 1
0	Page Mode Operation with 1Wait State
1	Page Mode Operation with Zero Wait State when Page Hit

D3-D2: CAS Precharge Time

D3	D2	PROCCLK Cycles
0	0	4
0	1	3
1	0	2
1	1	1

D1-D0: CAS Active Time

D1	D0	PROCCLK Cycles
0	0	4
0	1	3
1	0	2
1	1	1

CONTROL REGISTER 3 8 R/W bits at I/O address 1EF (Hex) Default Memory Size (A23-A16)
D7-D0 External Expansion Ram

D7-D0: External Expansion Ram

From 0 to 255 numbers of 64K segments before expansion memory should be decoded. For example 0 would indicate that all system board RAM should be disabled for all but EMS and shadow.

After /RESET will be 0.

CONTROL REGISTER 4 8 R/W Bits at I/O address 1EF (Hex) Reset State: 0	
D7-D4	Reserved
D3	Numeric Co-processor Select
D2	I/O Speed
D1	Interleave Mode
D0	Reserved

D7 - D4 Reserved

D3: I/O Speed

0	System clock is to be slowed down (8MHz) to accomodate off-board memory and peripherals (Default)
1	Full speed

D2: Numeric Co-processor Select

0	Numeric Co-processor exists
1	Numeric Co-processor does not exist (default)

D1: Interleave Mode

0	Word Interleave
1	Page Interleave

D0: Reserved

This Bit must be set to 0.

The following are features of Control Register 5.

Control Register 5 8 R/W bits at I/O address 1EF (Hex) Reset State: 0	
D7	Sleep Mode Enable
D6-D4	Frequency of Sleep Mode
D3-D0	Reserved

D7: Sleep Mode Enable

0	Normal (default)
1	Sleep Mode

D6-D4: Frequency of Sleep Mode

000	4MHz *
001	2MHz *
010	1MHz *
011	0.5MHz *
100	0.25MHz *

*These frequencies are referenced to asynchronous clock (CLKASN) signal running at 32 MHz.

D3-D0: Reserved

HT21
Interleave Addressing

The memory address multiplexers provide the proper address for the memory array. There are two types of interleaving available, word and page interleaving. When Control Register 4 is selected, bit D1=0 will select Word Interleave, bit D1=1 will select Page Interleave. Note: Interleaving can only occur when an even number of banks of memory have been installed on the system board.

Word 2-Way and 4-Way Interleaving selects the proper bank of memory by applying the proper /RAS and /CAS signal as selected by the RASA and RASB bits defined in the chart.

BK=Bank A=Address T=Translated Address (Bank and Translated Address are from A14-A23.

WORD INTERLEAVE												
		RASA	RASB	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
Memory Type 256K					(Mixed with 1M or Not)								
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A1	BK1	A10	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			BK0	A11	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A1	A2	A10	A11	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			BK0	BK1	A12	A13	T14	T15	T16	T17	T18	T20
Memory Type 1M					(Only)								
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A1	BK1	A11	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			BKO	T19	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A1	A2	A11	A12	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			BK0	BK1	T19	A13	T14	T15	T16	T17	T18	T20
256K with 64K					(Maximum Memory 640K)								
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	T17	T19
	RAS			A10	A11	A12	A13	T14	T15	T16	A9	T18	T20
Refresh													
N/C	RAS			A1	A2	A3	A4	A5	A6	A7	A0	A8	A9

Page Interleave is accomplished in a similar manner to previously shown inteleaving. The Page interleave chart showing the RASA and RASB signals and address translation is shown below. In Page Interleave mode, only 256K and 1Meg devices are supported. 256K devices will result in a 4K Page Size and 1Meg devices will result in a 8K page size.

PAGE INTERLEAVE

		RASA	RASB	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
MemoryType 256K					Mixed with 1M or Not No 64K)								
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A11	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	BK0	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A11	A12	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	BK0	BK1	A13	T14	T15	T16	T17	T18	T20
Memory Type 1 M					Only								
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A11	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	BK0	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A11	A12	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	BK0	BK1	A13	T14	T15	T16	T17	T18	T20

4 Way Word Interleave Addressing

4 BANKS 1M Devices

4 Way Interleave

DRAM 1 MWord (16 1M devices + 2 Parity)	DRAM 1 MWord (16 1M devices + 2 Parity)	DRAM 1 MWord (16 1M devices + 2 Parity)	DRAM 1 MWord (16 1M devices + 2 Parity)

— 8 MByte

— 4 MByte

— 0K

4 BANKS 256K Devices

4 Way Interleave

BANK 3	BANK 2	BANK 1	BANK 0
DRAM 512K Word (16 256K Devices +2 Parity)	DRAM 512K Word (16 256K Devices +2 Parity)	DRAM 512K Word (16 256K Devices +2 Parity)	DRAM 512K Word (16 256K Devices +2 Parity)
A2 = 1 = DBLWRD1		A2 = 0 = DBLWRD0	
16 Bit Word 3	16 Bit Word 2	16 Bit Word 1	16 Bit Word 0
Byte 7 | Byte 6	Byte 5 | Byte 4	Byte 3 | Byte 2	Byte 1 | Byte 0

— 2 MByte

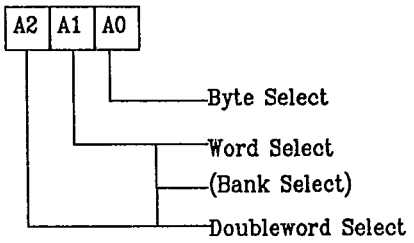
— 1 MByte

— 0K

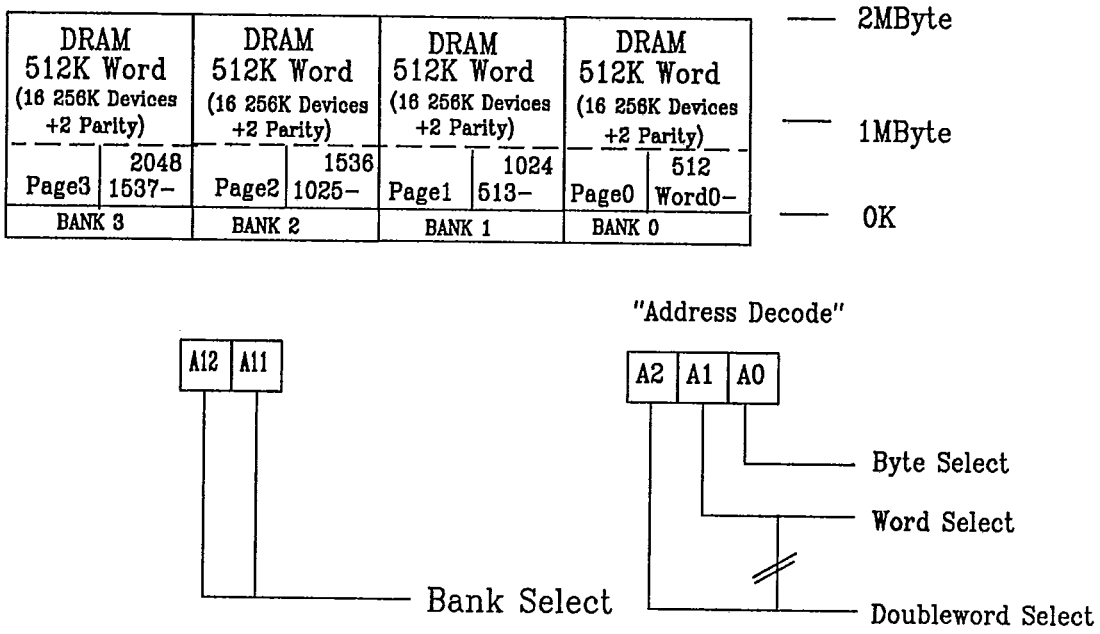
A1=Low=Even Word;A1=High=Odd Word

A0=Low=Even Byte;A0=High=Odd Byte

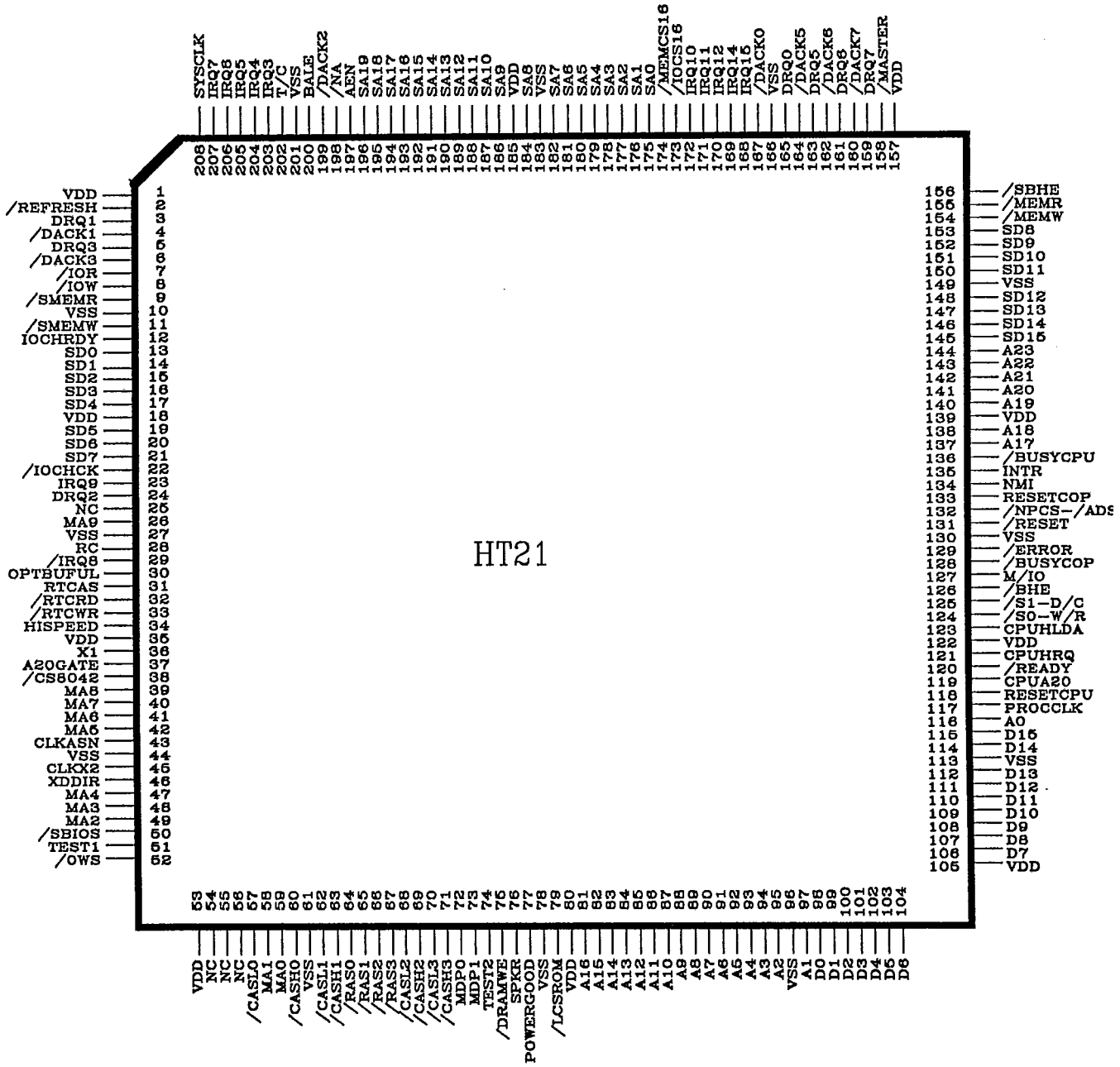
"Address Decode"



4 Way Page Interleave Addressing



HT21
Pin Diagram



Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
A0-A16	116,97 95-81	I	PU	Address bits 0-16: Inputs from 80286 CPU or 80386SX CPU. The HT21 takes the address bus inputs and generates SA bus for I/O slots, and the MA bus for the system DRAM.
A17-23	137,138,140-144	I/O	PU	A17-23, bi-directional Address lines: Inputs from the 80286 CPU or 80386SX CPU used for memory selection decoding. They output addresses from the memory mapper (internal) logic during DMA operations.
A20GATE	37	I		Gates address from CPU: If CPUHLDA=0 the CPU is driving the address bus. When A20GATE is high, the upper address bit (CPUA20 input) drives the A20 pin directly, when low the A20 output is forced low regardless of the state of CPUA20.
AEN	197	O		Address ENable DMA: This signal is used to disconnect the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When AEN is high, the DMA controller drives the address bus, data bus, I/O read/write lines and memory read/write signals.
BALE	200	O		Buffered Address Latch Enable: This signal is provided by the 82288 bus controller and is used to latch valid addresses and memory decodes from the microprocessor. It is used by the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). A high level indicates the presence of valid address at the I/O slots. System Addresses (SA0-19) are latched on the falling edge of BALE.
/BHE	126	I	PU	Byte High Enable: A low at this input enables the high byte (15-8) of the data bus. Driven by the CPU.
/BUSYCOP	128	I	PU	/BUSYCOP input to be connected to /BUSY output of the coprocessor. When the math co-processor is working, it drives this pin low, which in turn forces /BUSYCPU output low and halts the CPU.
/BUSYCPU	136	O		/BUSYCPU output connects to the /BUSY input of the CPU. A low level on this pin indicates the math co-processor is operating. Interrupts are honored by the CPU while this input is low. (See /ERROR)

* Indicates Internal Resistor

HT 21
Pin Description

Pin Symbol	Pin Num-bers	Pin Type	Pull Up/Dn*	Description
/CASH0- /CASH3	60,63,69,71	O		Column Address Strobe High order byte: Control up to four banks of DRAMs.These signals can be connected directly to DRAM CAS inputs through a 22 Ohm resistor.
/CASL0- /CASL3	57,62,68,70	O		Column Address Strobe Low order byte: Controls up to four banks of DRAMs. These signals can be connected directly to DRAM CAS inputs through a 22 Ohm resistor.
CLKASN	43	I	PU	CLocKASN: Drive this clock input at four times the desired SYSCLK frequency. This signal is used when CPU running at "Low" speed. For 16MHz system operations CLKX2 and CLKASN can share the 32 MHz OSC.
CLKX2	45	I	PU	CLocK X 2: Drive this clock input at twice the desired processor clock (PROCCLK) frequency. This signal is used when CPU is running at "High" speed. For 16MHz system operations CLKX2 and CLKASN can share the 32MHz OSC.
CPUA20	119	I	PU	CPU Address 20 from CPU: This input drives the A20 output pin, if CPUHLDA = 0 and A20GATE = 1.
CPUHLDA	123	I	PD	CPU Hold Acknowledge: The CPU drives this input high to indicate that it has released control of the buses.
CPUHRQ	121	O		CPU Hold ReQuest: When high, the HT21 needs to perform a DMA, Refresh, or bus Master operation.
/CS8042	38	O		Chip Select 8042: A low level drives /CS of an external keyboard controller.
D0-D15	98-104,106- 112, 114, 115	I/O	PU	Bi-directional Data Bus: Data to/from the CPU.
/DACK0-3 /DACK5-7	167,4, 199,6,164,162 160	O		DMA ACKnowledge: When low, these signals are used to acknowledge DMA requests (DRQ0-3,5-7) from peripherals on the I/O expansion slots.

* Indicates Internal Resistor

Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
/DRAMWE	75	O		DRAM Write Enable: Generates the write strobe to DRAMs. This is a gated signal derived from the /MEMW input.
DRQ0-3, DRQ5-7	165,3,24,5, 163,161,159	I	PD	DMA ReQuests: These asynchronous channel requests are used by peripheral devices and the I/O channel microprocessors, active high signals request DMA services or control of the system. They are prioritized with DRQ0 having the highest priority and DRQ7 having the lowest. Each signal should be held high until the corresponding DMA Request Acknowledge (/DACK signal) goes active (low). DRQ0-3 govern 8-bit DMA transfers, DRQ5-7 control 16-bit DMA transfers with devices on the I/O slots.
/ERROR	129	I	PU	ERROR: Connect /ERROR from the co-processor to this input. A low level indicates the math co-processor has an unmasked error condition.
HISPEED	34	I	PU	HIgh SPEED: When high, PROCCLK (the processor clock) speed is equal to the CLKX2 rate for on-board memory accesses. When low, PROCCLK is one half of CLKASN.
INTR	135	O		INTerrupt Request: A high on this output requests an interrupt from the CPU.
/IOCHCK	22	I	PU	I/O CHannel CheckK: A low on this input indicates there is an uncorrectable system error. Provides the system board with parity (error) information about memory or devices on the I/O channel. This causes the NMI (Non-Maskable Interrupt) output to become active (high), and interrupts the CPU. Needs external pullup.
IOCHRDY	12	I/O	PU	I/O CHannel ReaDY: Held low by the HT21 to lengthen the cycles by an integral number of clock cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read/Write command. The HT21 will add more wait states for a page miss by pulling this signal low. Needs external pullup.

* Indicates Internal Resistor

HT21
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
/IOCS16	173	I	PU	I/O Chip Select 16: A low indicates a 16-bit data transfer on the SA bus. This signal should be driven by an open collector or tri-state driver capable of sinking 20mA. Needs external 300 Ohm pullup.
/IOR	7	I/O	PU	I/O Read: When low, instructs an I/O device to drive its data onto the data bus. It is driven by the microporcessor or DMA controller, either resident in the system or on the I/O channel.
/IOW	8	I/O	PU	I/O Write: When low, instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system.
IRQ3-7, IRQ9-12, IRQ14-15	203-207,23, 172-170,169,168	I	PU	Interrupt ReQuest: These pins signal the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). IRQ3 has the highest priority interrupt, IRQ15 the lowest.
/IRQ8	29	I	PU	This input is driven by a Real Time Clock interrupt output. (Note that Interrupt Request 8 is active low,unlike the other Interrupt Requests.)
/LCSROM	79	O		Latch Chip Select ROM: Drives the chip enable pins of the EPROM, ie E0000-FFFFF and FE0000-FFFFFF for EPROMs.
M/IO	127	I	PU	Memory I/O: From CPU: if high during set up, memory cycle is in progress; if low, I/O cycle is occuring. Tri-state when the CPU is in Hold Acknowledge. (See CPUHLDA)
MA0-MA9	59,58,49-47,42-39,26	O		Multiplexed Address bus: to DRAMs, should connect to the memory address of the DRAM through 22 Ohm resistors.

* Indicates Internal Resistor

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
/MASTER	158	I	PU	/MASTER: This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel issues a DRQ to a DMA channel in cascade mode and receives a /DACK. Upon receiving the /DACK, an I/O microprocessor pulls /MASTER input low, which will allow it to control the system address, data, and control lines. After this signal is pulled low the I/O microprocessor must wait one system clock period before driving the address and data lines and two clock periods before issuing a Read/Write command. If this signal is held low for more than 15 microseconds, the system memory may be lost because of a lack of refresh.
MDP0 MDP1	72,73	I/O	PU	Memory Data Parity: Low (0) and high (1) bytes: When data is written to RAM or read from RAM its parity value is calculated.
/MEMCS16	174	I	PU	EXternal MEMory Chip Select 16 wide: External devices drive this input low for 16-bit data transfers. Connects to the system expansion bus. Needs external 300 Ohm pullup.
/MEMR	155	I/O	PU	MEMory Read signal: Output is low during a memory read cycle. This signal instructs the memory devices to drive data onto the data bus. It can be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel drives this signal it must have the address lines valid on the bus for 1 system clock period before driving /MEMR active. Tri-stated when MASTER is low and the CPU does not control the system. Not active during local memory cycles.
/MEMW	154	I/O	PU	MEMory Write signal: Output is low during a memory write. This signal instructs the memory devices to store the data present on the data bus. It is active during all memory read cycles and can be driven by any microprocessor or DMA controller in the system. When driven by a microprocessor on the I/O channel the address lines on the bus must be valid for one system clock period before driving the signal active. This is tri-stated when MASTER is low. Not active in local memory cycles.
/NA	198	O		Next Address: This is used to except Address Pipelining even if the end of the current cycle is not acknowledged with a /READY. 0 = Pipeline mode, 1 = non-pipeline mode (default).

* Indicates Internal Resistor

HT21
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
NMI	134	O		Non-Maskable Interrupt: A high level forces the CPU to unconditionally execute an interrupt routine.
/NPCS-/ADS	132	I/O	PU	Multiplexed /NPCS and /ADS operations, depending on auto-sense definition of mode. Input /ADS, when 386SX mode is selected (Mode=0). /ADS: ADdress Status input from the 386SX. When low, the 386SX is providing valid address on A23-A1, and driving the R/W, D/C, M/IO, /BHE, A0 control lines. Output /NPCS, when 286 operation is selected (Mode=1). /NPCS: Numeric Processor Chip Select. A low output enables the co-processor chip.
OPTBUFUL	30	I	PD	OutPuT BUffer FULl: Input from P24 of the keyboard controller. Setting this pin high activates the internal IRQ. This causes an INTR to the CPU, indicating the keyboard buffer is full.
POWERGOOD	77	I	PU	POWERGOOD: When low, it resets the HT21 controller. A Schmitt Trigger buffers the input pin.
PROCCLK	117	O		PROCessor CLocK: this output supplies the clock signal for the CPU and co-processor. It drives CLK on the CPU, and the clock lines on the co-processor. Rate determined by HISPEED.
/RAS0- /RAS3	64-67	O		Row Address Strobe: Controls up to four banks of DRAMs. These signals can be connected directly to DRAM RAS inputs through a 22 Ohm resistor.
/RC	28	I	PU	Reset CPU: When driven low by the keyboard controller (P20), the CPU resets its internal registers.
/READY	120	O		READY: A low level tells the CPU that the current bus cycle is near completion.
/REFRESH	2	I/O		REFRESH: Input is low when the current cycle is for memory refresh and can be driven by a microprocessor on the I/O channel. Needs external pullup.

*Indicates Internal Resistor

HT21
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
/RESET	131	O		RESET: A low level used to reset the system logic at power-up or low-line voltage. (Open Drain Outputs)
RESETCOP	133	O		RESET COP: A high signal resets the co-processor.
RESETCPU	118	O		RESET CPU: A low-to-high transition resets the CPU during powerup, keyboard reset, and shutdown status. The rising edge resets the CPU, if the pin is held high for 16 clock cycles.
RTCAS	31	O		Real Time Clock Address Strobe: When low, this latches the RAM address for read/write operations.
/RTCRD	32	O		Real Time Clock ReaD: When low, data is read from the RTC.
/RTCWR	33	O		Real Time Clock WRite: When low, data is written to the RTC.
/S0-W/R	124	I	PU	Multiplexes /S0 and W/R functions, depending on auto-sense mode selection. Input W/R, when 386SX support (mode = 0). W/R: Write or Read bus cycles of the 386SX high for Writes, low for Reads. Input /S0 when 286 operation (mode = 1). 286 CPU Status bit. When /S0, /S1, INTA are low and M/IO is high - a shutdown or halt of the 286 occurs. If A1 =1, the CPU shuts down. If A1 = 0, the system shuts down.
/S1-D/C	125	I	PU	Multiplexes /S1 and D/C functions, depending on auto-sense mode selection. Input D/C, when 386SX support (mode = 0). D/C: Data or Control bus cycles. A high level indicates a Memory or I/O Data cycle by the 386SX. Low indicates a control cycle; inclusively interrupt acknowledge, halt, or code fetches. Input /S1 when 286 operation (mode = 1). 286 CPU Status bit. (See /S0-W/R)
SA0	175	I/O	PU	System Address bit 0: Bi-directional address bit on the expansion slot. It supplies address bit 0 during refreshes.

* Indicates Internal Resistor

HT21
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
SA1-SA19	176-182,184,186-196	I/O	PU	System Address bus: Bi-directional bus used to address memory and I/O devices within the system. These lines allow access of up to 16 MB of memory. SA0-19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.
/SBHE	156	I/O	PU	System Byte High Enable: Low when peripherals are performing a transfer on the upper byte. Sixteen-bit devices use /SBHE to condition data bus buffers tied to SD8 - SD15.
/SBIOS	50	I	PU	Switch for single BIOS: 1 = Two Chip BIOS 0 = Single BIOS
SD0-15	13-17,19-21 153-150,148-145	I/O	PU	I/O System Data Bus: These signals provide bus bits 0-15 for the microprocessor, memory, and I/O devices. SD0 is the least-significant bit and SD15 is the most significant bit. All 8- bit devices on the I/O channel should use SD0-SD7 for communications to the microprocessor. The 16-bit devices will use SD0-SD15. To support 8-bit devices, the data on SD8-SD15 will be gated to SD0-SD7 during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.
/SMEMR	9	O		System MEMory Read: Low during memory reads. This signal instructs the memory devices to drive data onto the data bus. It is active only when the memory decode is within the low 1MB of memory space. This is a buffered version of /MEMR.
/SMEMW	11	O		System MEMory Write: Low during memory writes. This signal instructs the memory devices to store the data present on the data bus. It is active only when the memory decode is within the low 1 MB of memory space. This is a buffered version of /MEMW.
SPKR	76	O		SPeaKeR: Output of the Timer 8254 Channel 2 (mega function). This connects to a speaker, through a buffer.

* Indicates Internal Resistor

HT 21
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Pull Up/Dn*	Description
SYSCLK	208	O		SYStem CLocK: This provides a clock for devices on the expansion slot. SYSCLK is a quarter of CLKASN.
TC	202	O		Terminal Count: pulses high when the DMA channel terminal count is reached. This signal is available on the expansion slot.
TEST 1, TEST 2	51,74	I	PU	Tie TEST1 and TEST2 low (0) to tri-state all outputs. If not using the tri-state feature these pins should not be used or connected.
X1	36	I	PU	This input is tied to a 14.31818 MHz Oscillator, to generate OSC.
XDDIR	46	O		External Data BUS control for KBD and RTC, /SBIOS: 1 = Write 0 = Read
/0WS	52	I	PU	Zero Wait State: This signal tells the microprocesser that it can complete the present bus cycle without inserting additional wait cycles. It comes from an address decode gated with a Read/Write command. In order to run a memory cycle to an 8-bit device with a minimum of 2 wait states, 0WS must be driven low one system clock after Read/Write commands are gated with the address decode for the device. These Read/Write commands are active on the falling edge of the system clock. This signal should be driven by an open collector or tri-state driver capable of sinking 20mA. External 300 Ohm pull up.
VDD	1,18,35,53,80 105,122 139,157,185			Power: +5 Volts
VSS	10,27,44,61, 78,96,113,130 149,166,183, 201			Ground
NC	25, 54-56			Reserved

* Indicates Internal Resistor

All Inputs are TTL - voltage compatible, except where noted otherwise.

HT21
DC Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	+10	mA
Storage Temperature Range (Plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Ambient Temperature Range Commercial	TA	0 to +70	C

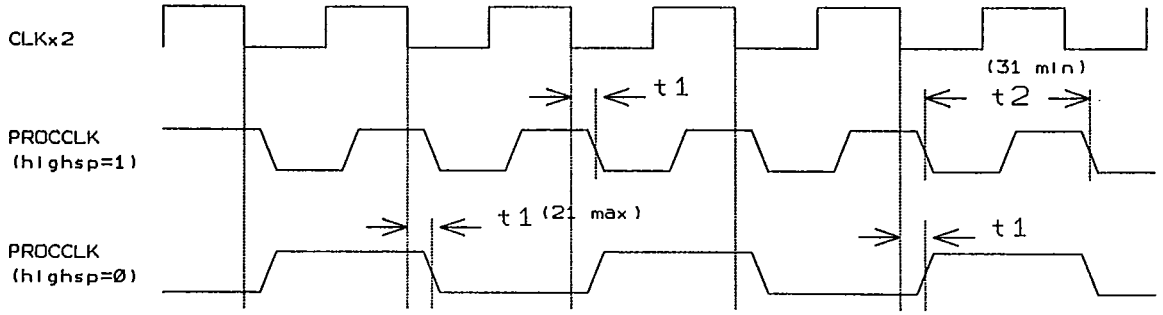
DC Characteristics: VDD = 5V +/- 5%, TA = 0 C to 70 C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input LOW	VIL				0.8	V
Voltage Input HIGH	VIH		2			V
Input Current	IIN		-10	+1	+10	uA
Voltage Output High	VOH		2.4	4.5		V
SD0-15, MA0-9, /RAS0-3, /DRAMWE		IOH=-12mA				
/CASL0-3, /CASH0-3, MDP0,1 PROCCLK		IOH=-8mA				
SPKR,/LCSROM, RESETCPU, /READY, CPUHRQ, /RESET, /NPCS-/ADS, RESETCOP, INTR, /BUSYCPU, /DACK0-3,5-7, /CS8042, RTCAS,/RTCWR, /RTCRD		IOH=-4mA				
All Others		IOH=-6mA				
Voltage Output LOW	VOL			0.4	0.8	V
SD0-15, MA0-9, /RAS0-3, /DRAMWE, SA0-19		IOL=24mA				
/CASL0-3, /CASH0-3, MDP0,1 PROCCLK		IOL=16mA				
SPKR,/LCSROM, RESETCPU, /READY, CPUHRQ, /RESET, /NPCS-/ADS, RESETCOP, INTR, /BUSYCPU, /DACK0-3,5-7, /CS8042, RTCAS,/RTCWR, /RTCRD		IOL=6mA				
All Others		IOL=12mA				
3-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	+1	10	uA
Output Short Circuit Current	IOS	VDD=Max,V0=VDD	20	110	220	mA
		VDD=Max,VO=OV	-10	-90	-190	mA
Supply Current	IDD	CLK=16MHz,CL=50pf		50		mA

Note: Not more than one output may be shorted at a time for a maximum duration of one second.

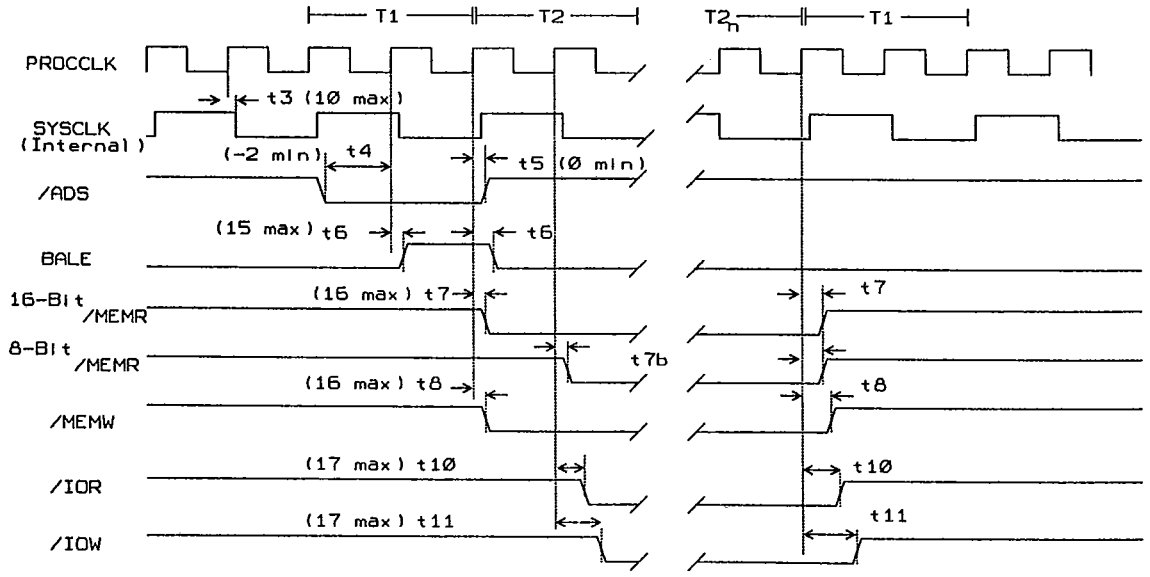
CLOCK TIMING

SX Mode



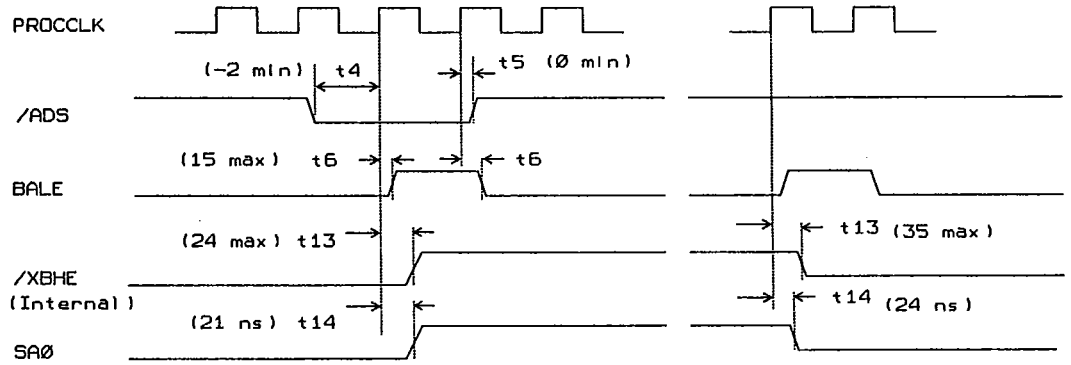
CONTROL SIGNAL TIMING

SX Mode



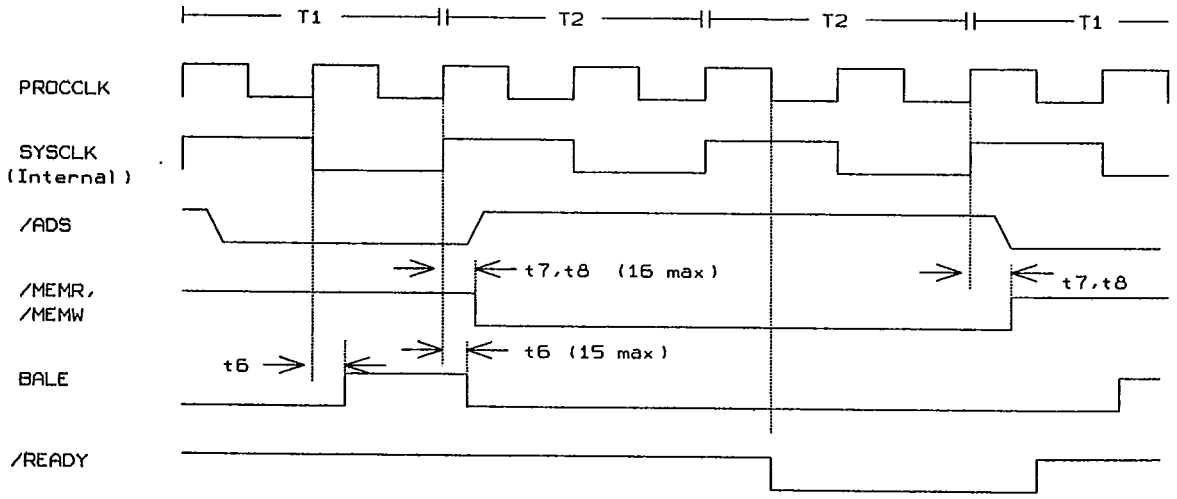
OUTPUT SIGNALS

SX Mode



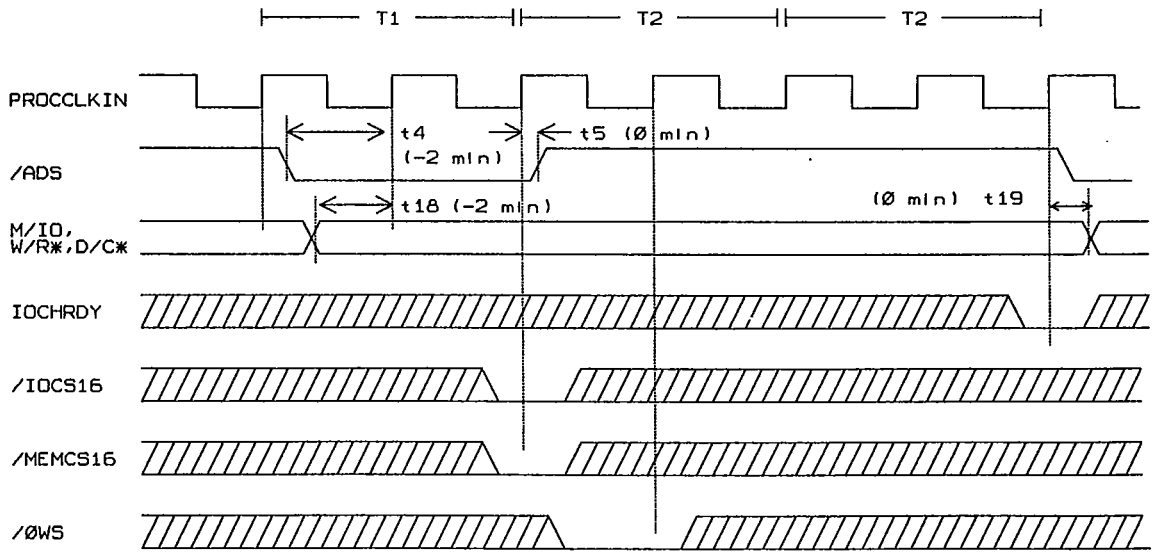
16 BIT MEMORY ACCESS (RAM) 1 WAIT STATE I/O BUS

SX Mode



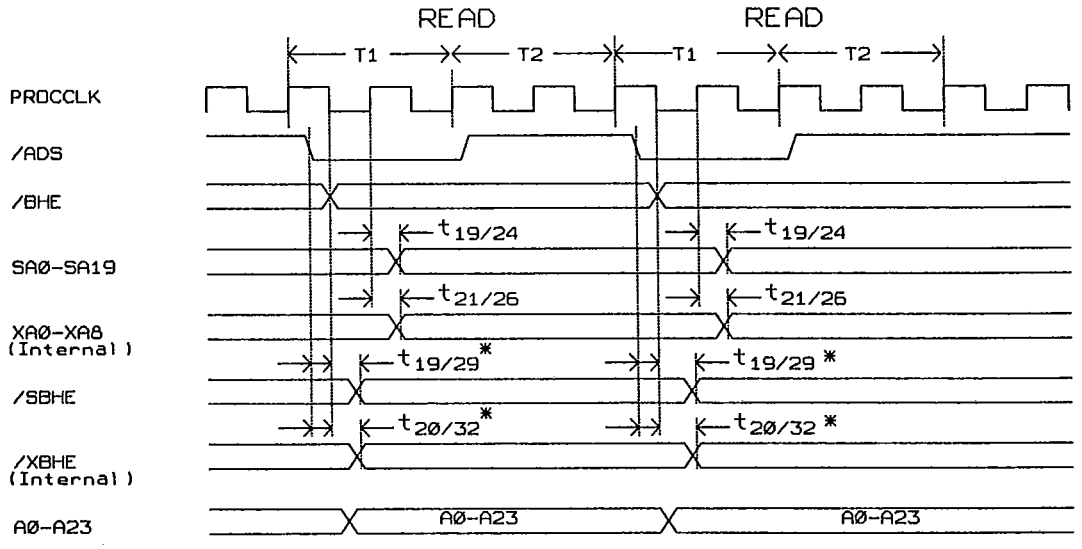
INPUT TIMING

SX Mode



NORMAL OPERATION, ADDRESS OUTPUT

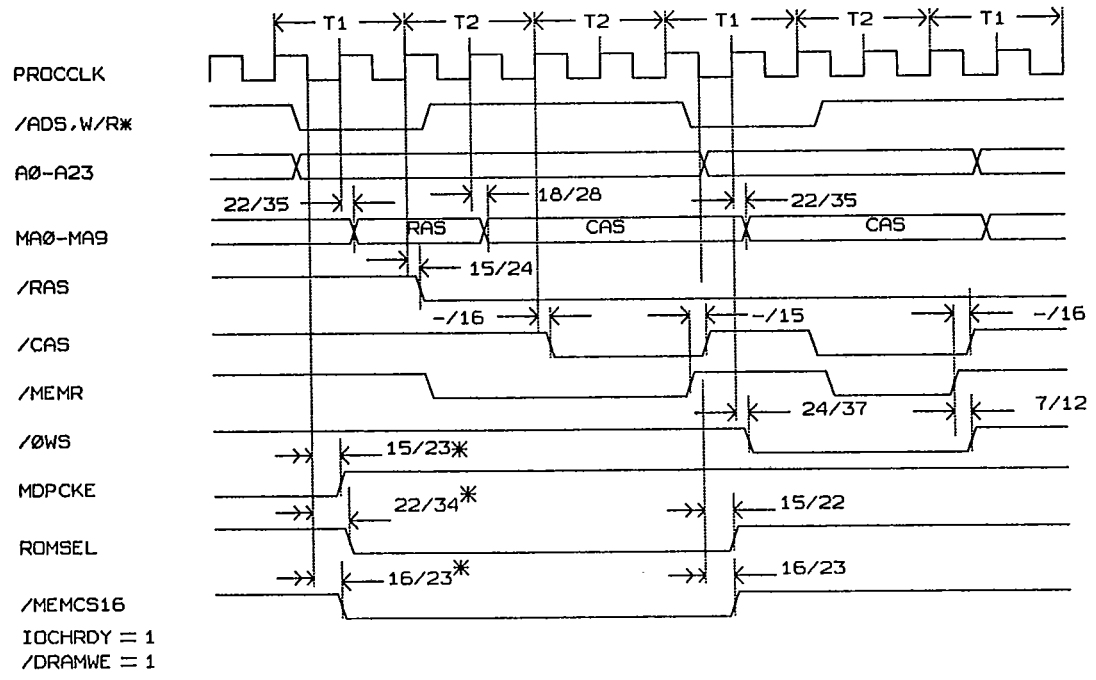
SX Mode



NOTE: TYPICAL/MAX DELAY
RELATIVE TO LATER OF 3 EDGES
*(PROCCLK FALLING, /ADS,or /BHE)

PAGE MODE, READS

SX Mode

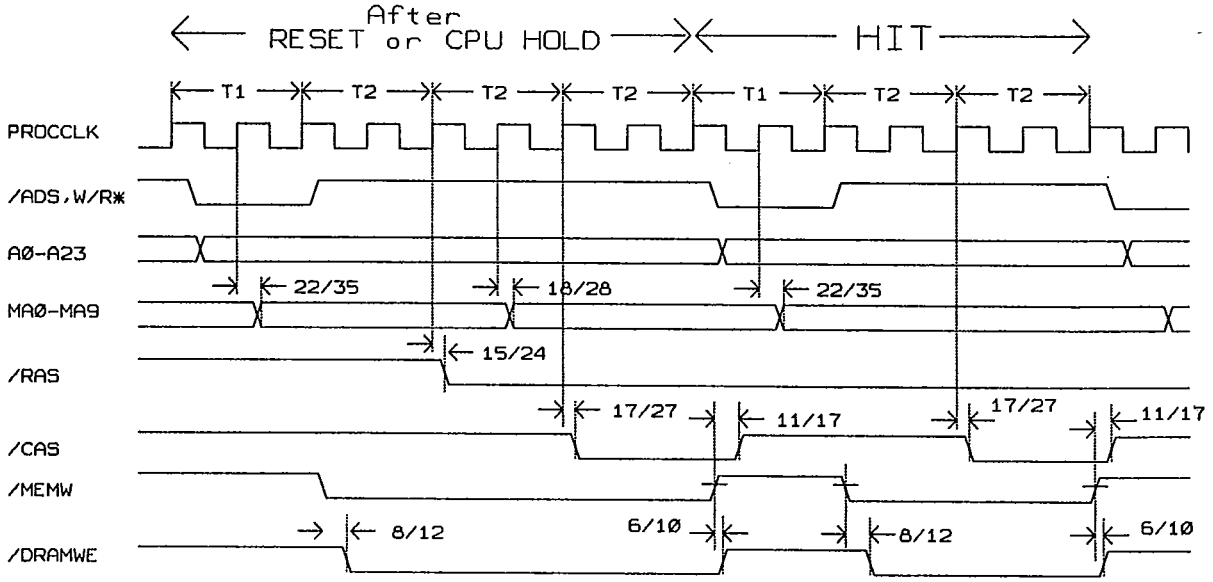


TYP/MAX DELAY, REL. TO LATER OF:
R = (PROCCLK RISING OR ADS)
F = (PROCCLK FALLING OR ADS)

PAGE MODE, WRITES - 1 WAIT STATE

SX Mode

Top of figure

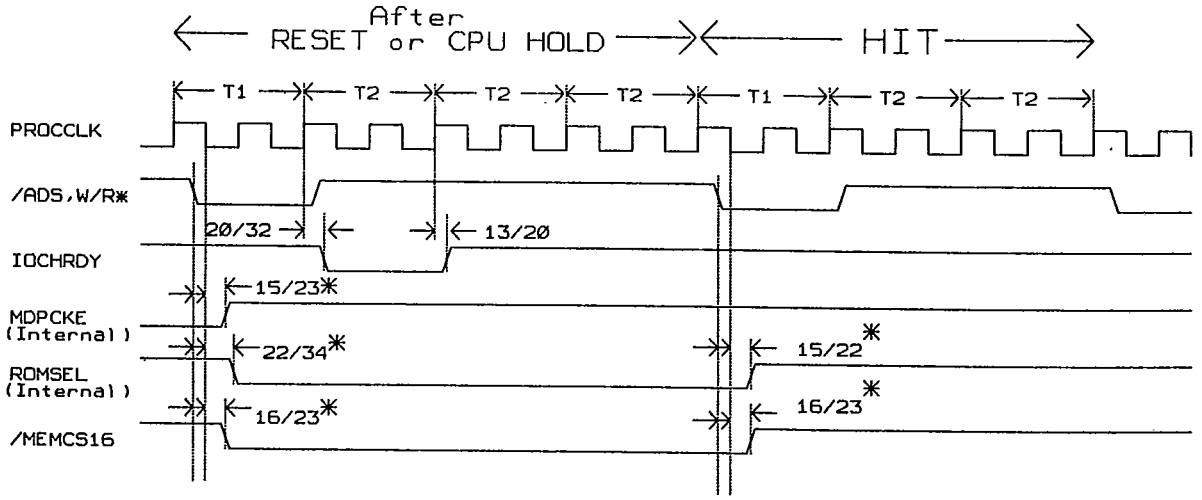


NOTE: TYP/MAX TIMINGS

PAGE MODE, WRITES - 1 WAIT STATE

SX Mode

Bottom of figure

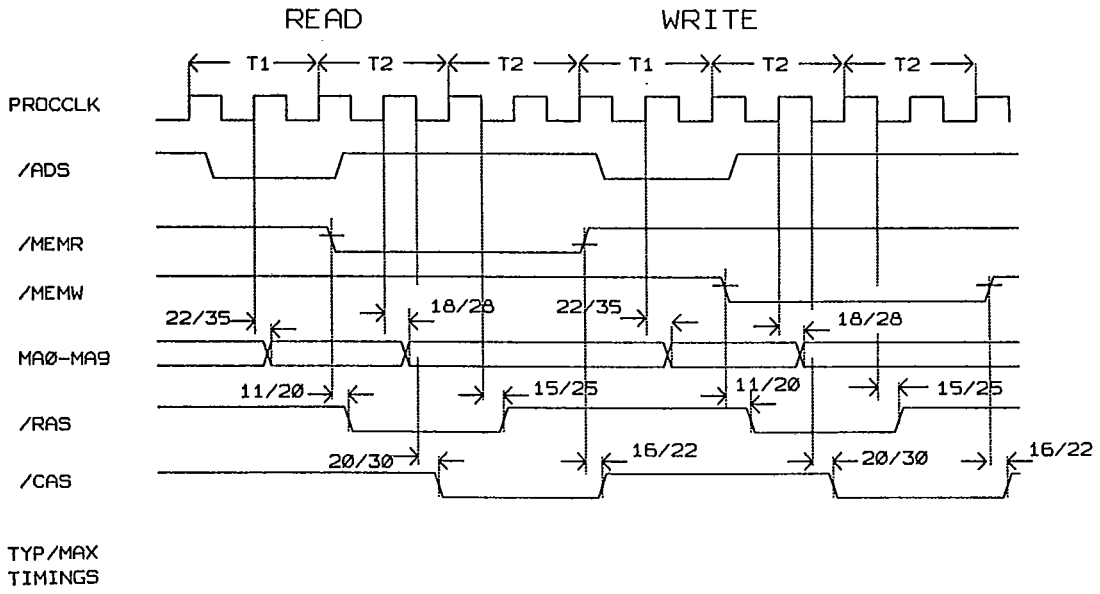


/0WS = 1

*NOTE: TYP/MAX TIMINGS
RELATIVE TO LATER OF 2 EDGES
(PROCCLK FALLING OR /ADS)

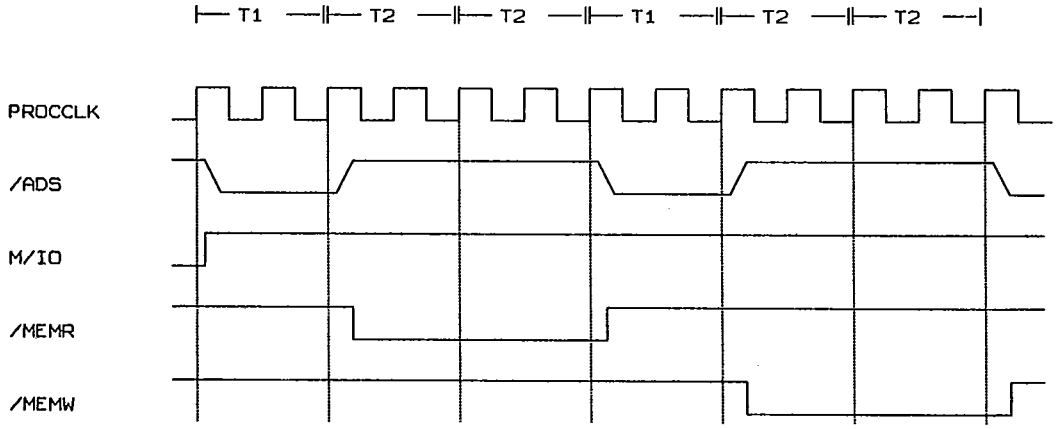
INTERNAL DELAY TIMING - 1 WAIT STATE

SX Mode



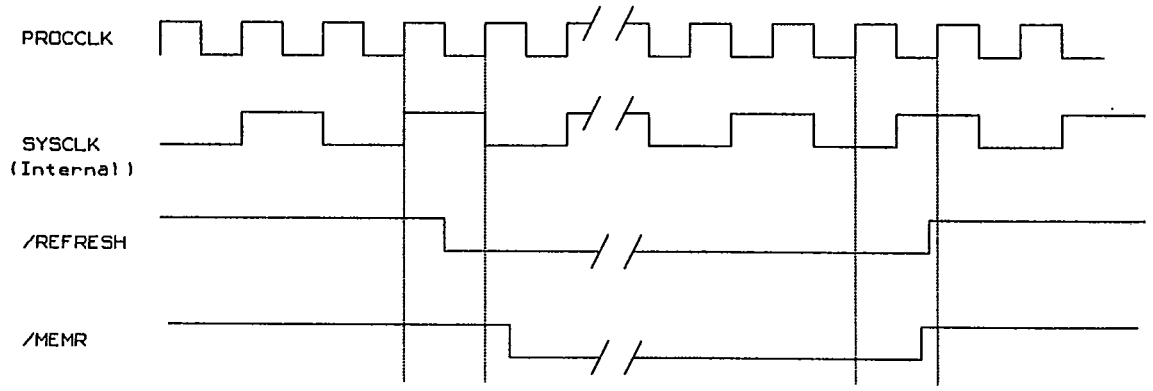
READ THEN WRITE, MEMORY CYCLE

SX Mode



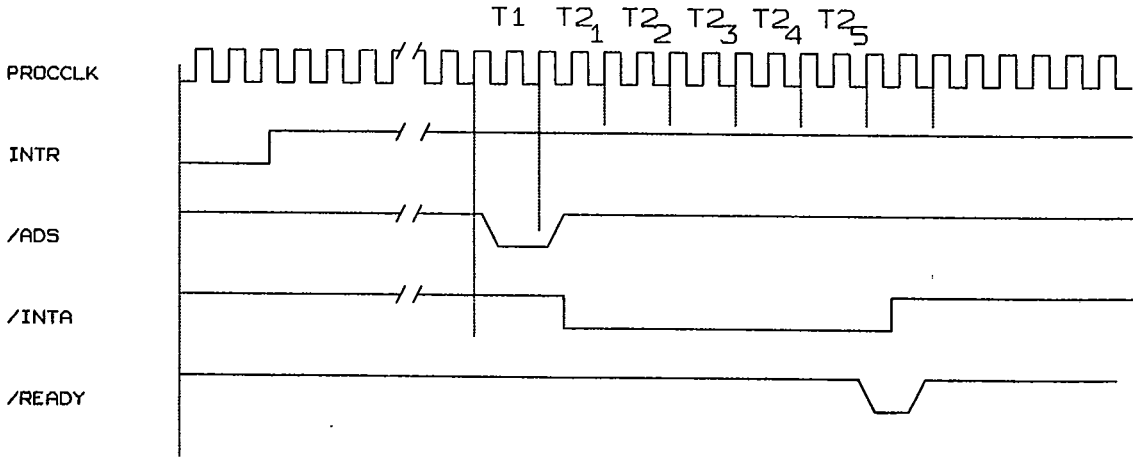
REFRESH TIMING

SX Mode



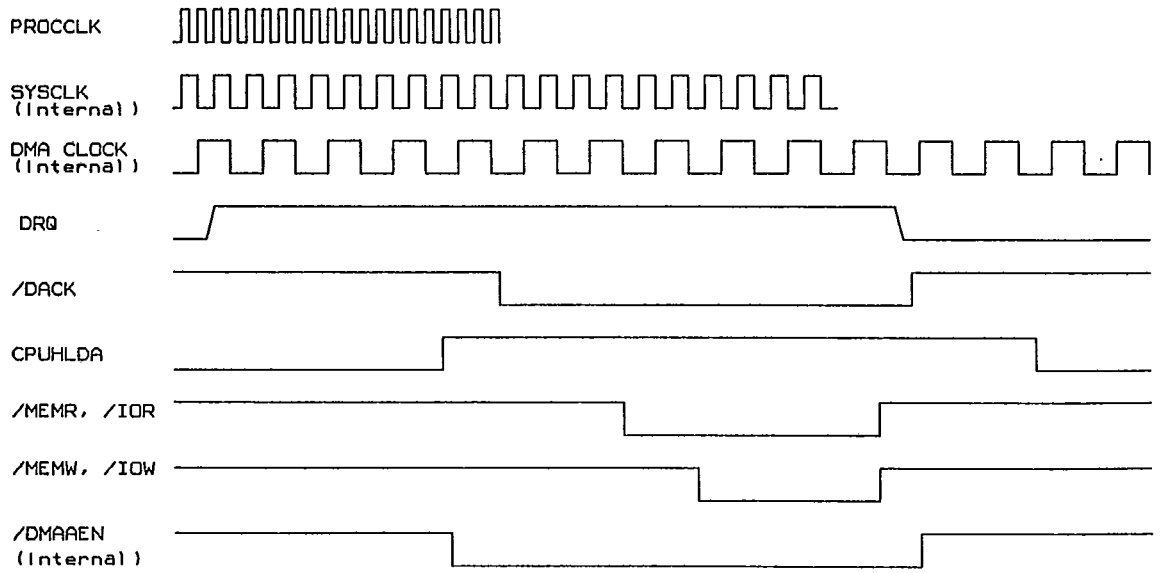
INTERRUPT TIMING

SX Mode



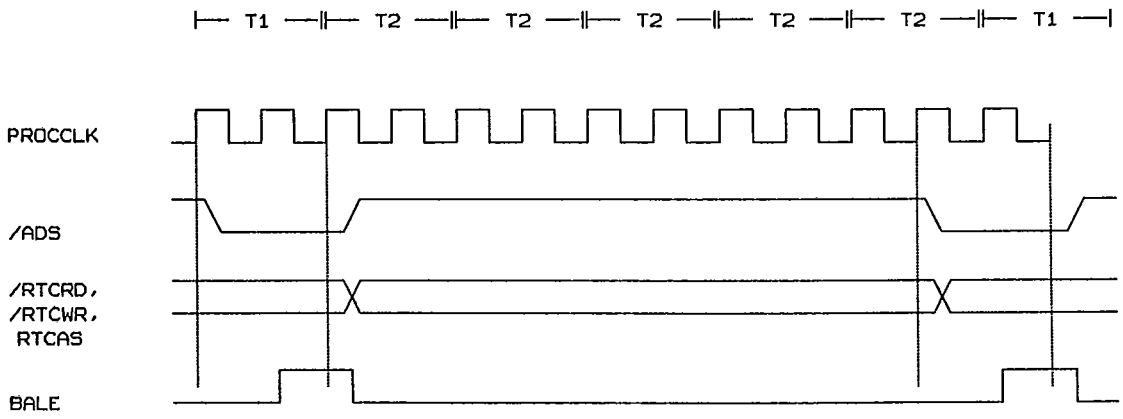
DMA ACKNOWLEDGE

SX Mode



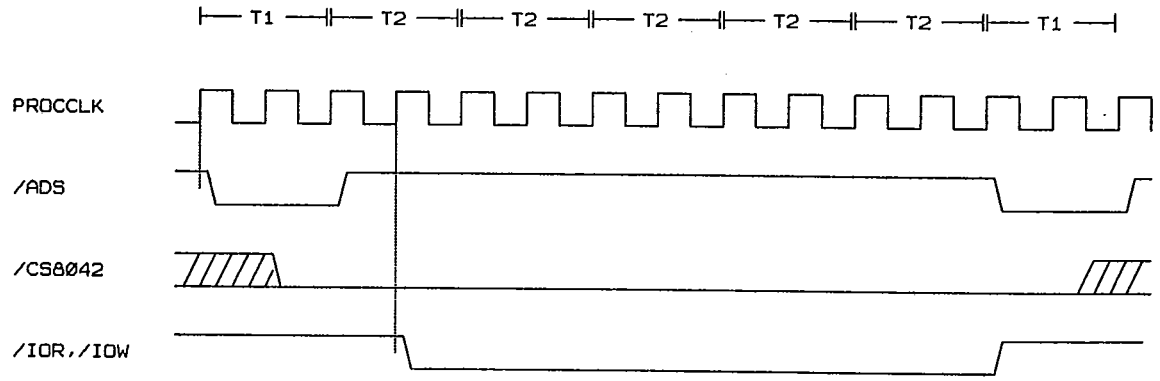
REAL TIME CLOCK ACCESS

SX Mode



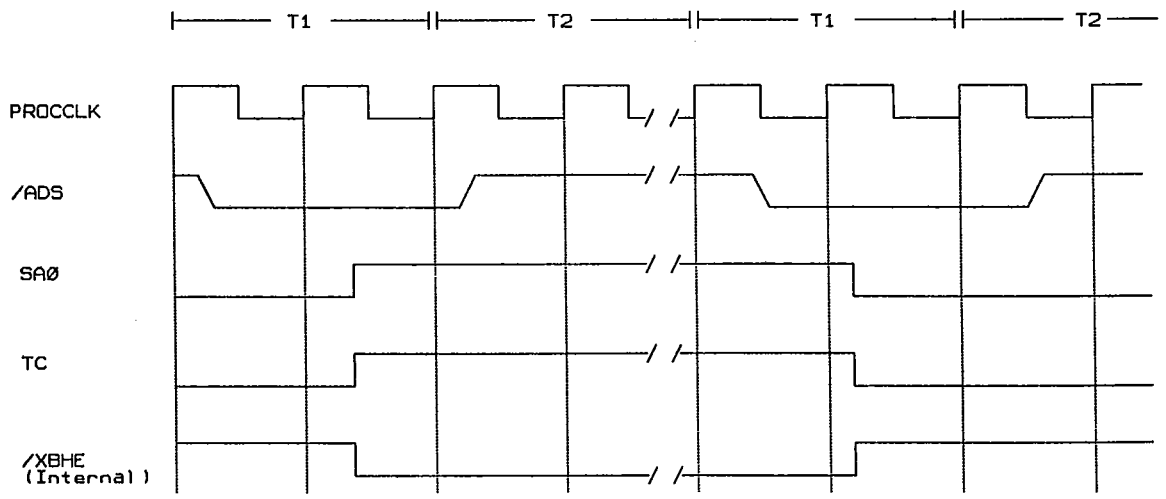
KEYBOARD CONTROLLER I/O TIMING

SX Mode



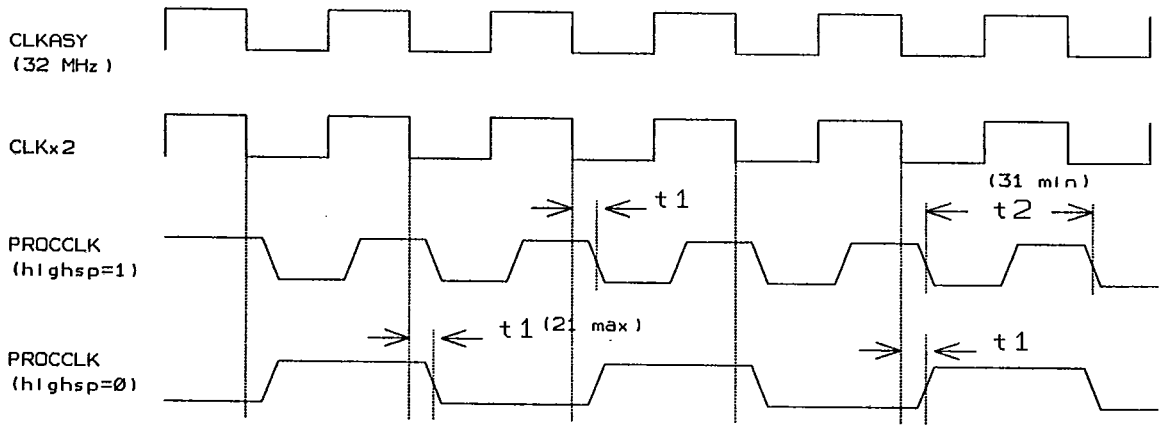
SA0, TC, /XBHE TIMING

SX Mode



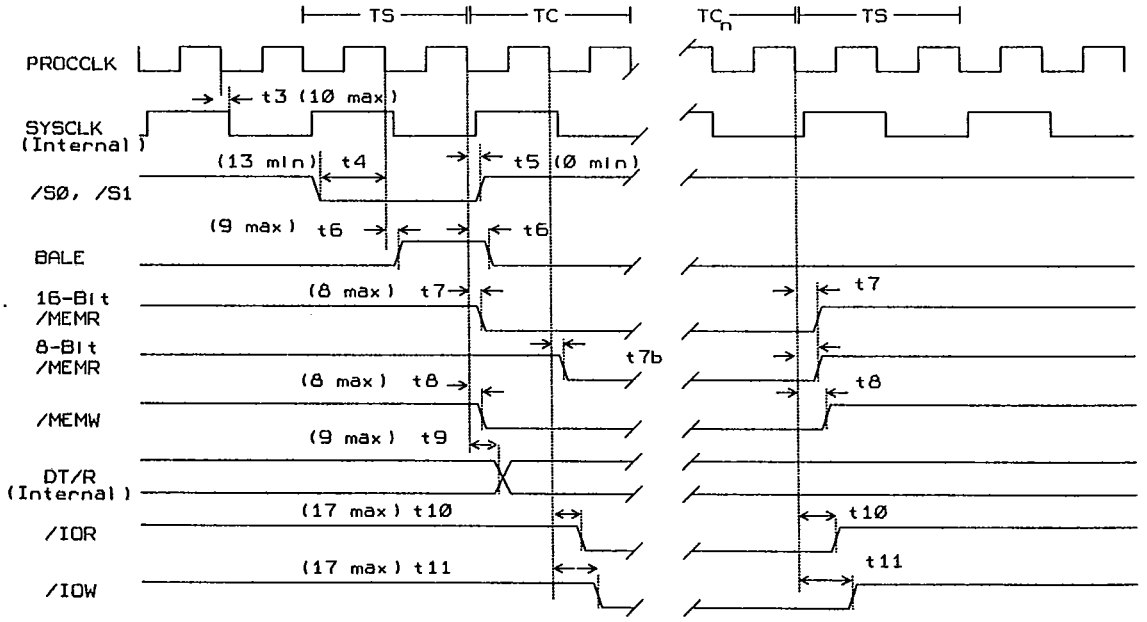
CLOCK TIMING

286 Mode



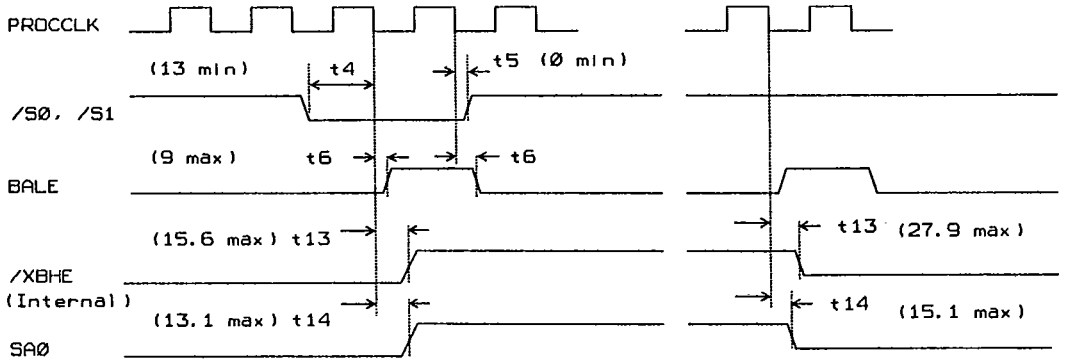
CONTROL SIGNAL TIMING

286 Mode



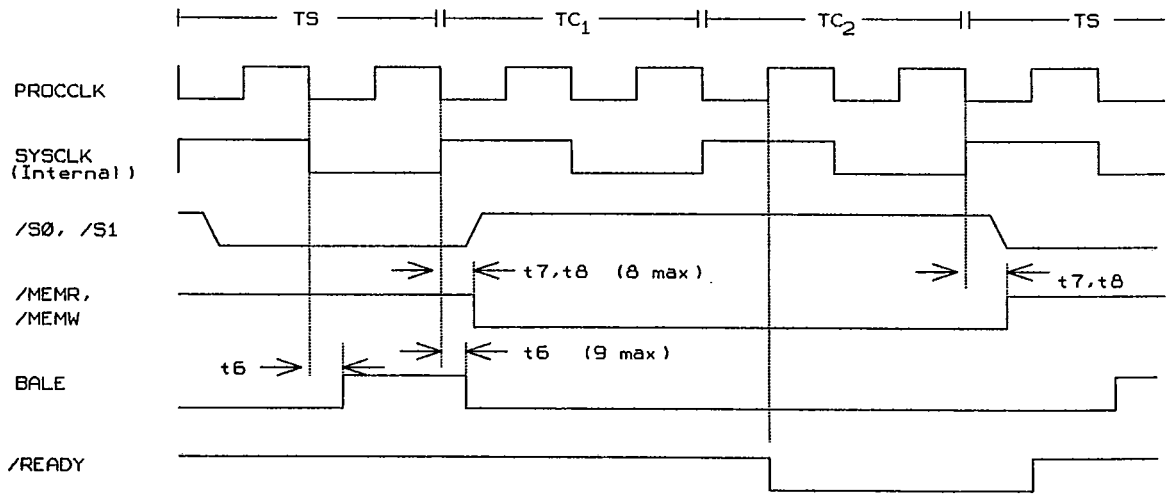
OUTPUT SIGNALS

286 Mode



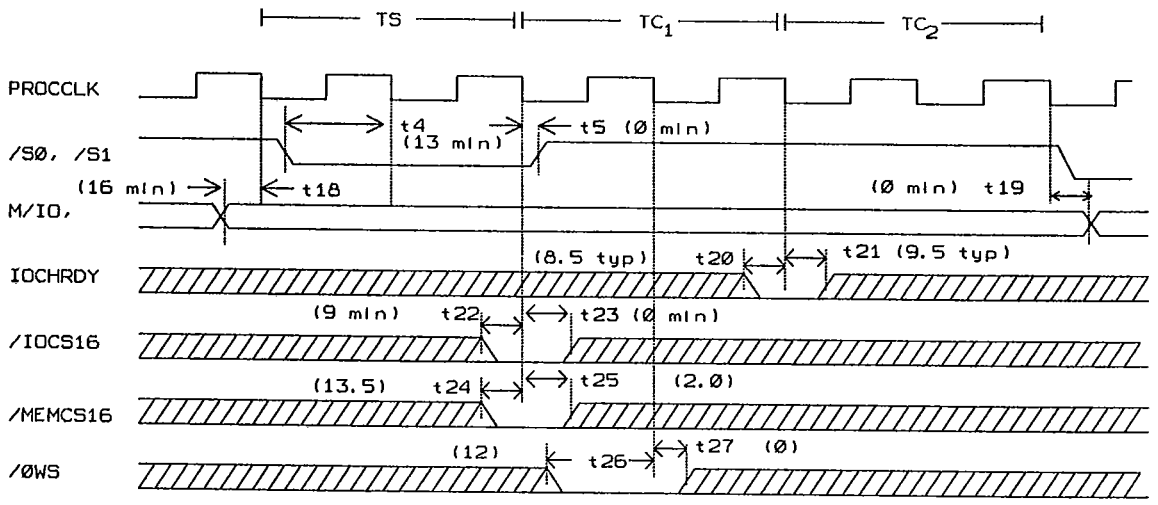
16 BIT MEMORY ACCESS (RAM) 1 WAIT STATE I/O BUS

286 Mode



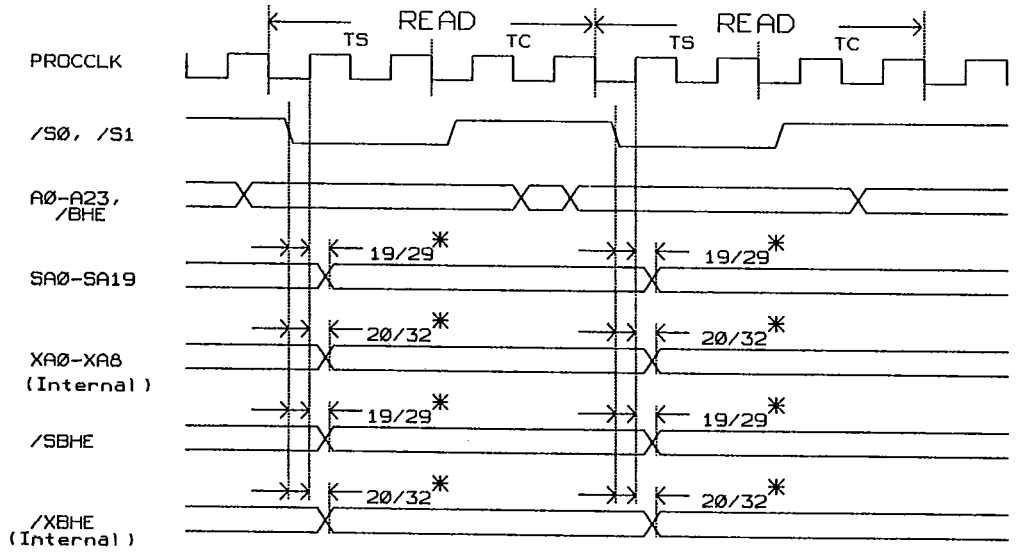
INPUT TIMING

286 Mode



NORMAL OPERATION, ADDRESS OUTPUT

286 Mode

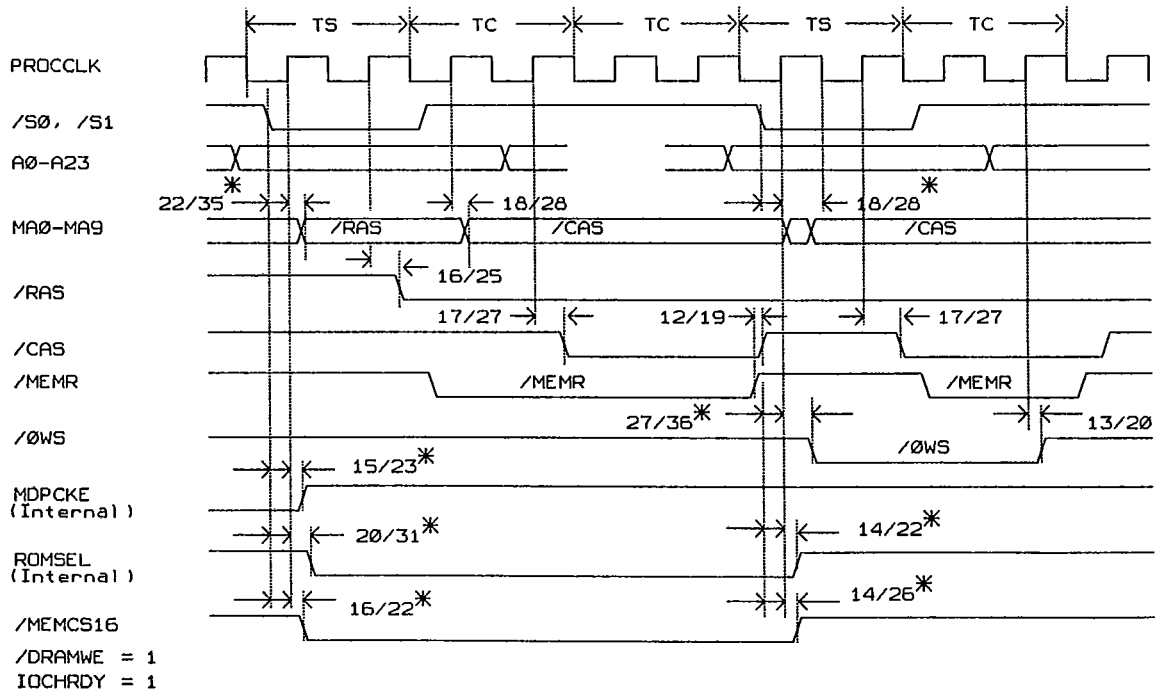


NOTE:

TYPICAL/MAX DELAY
RELATIVE TO LATER OF 2 EDGES
* = (PROCCLK RISING & S0*/S1*)

PAGE MODE, READS

286 Mode

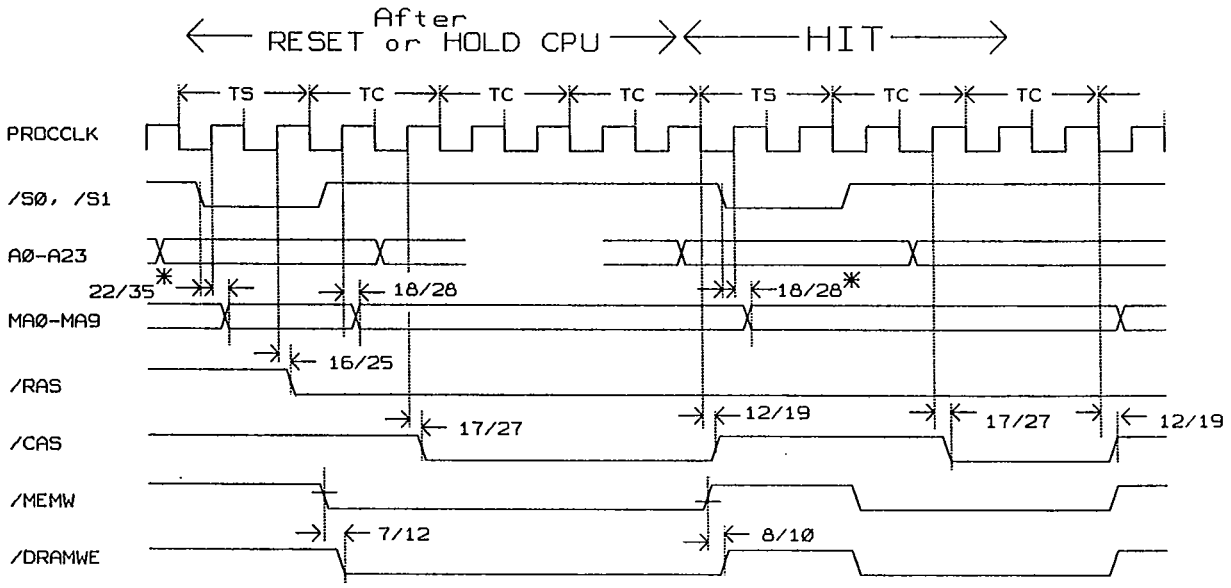


TYP/MAX DELAY, REL TO LATER OF:
(PROCCLK RISING OR S0*/S1*)

PAGE MODE, WRITES

286 Mode

Top

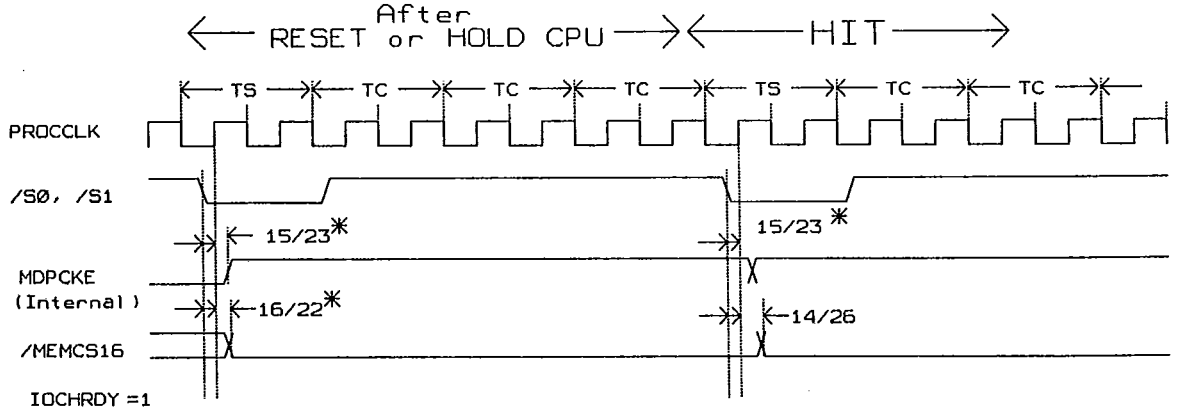


* NOTE: TYP/MAX TIMINGS
RELATIVE TO LATER OF 2 EDGES
(PROCCLK RISING or S0*/S1*)

PAGE MODE, WRITES

286 Mode

Bottom

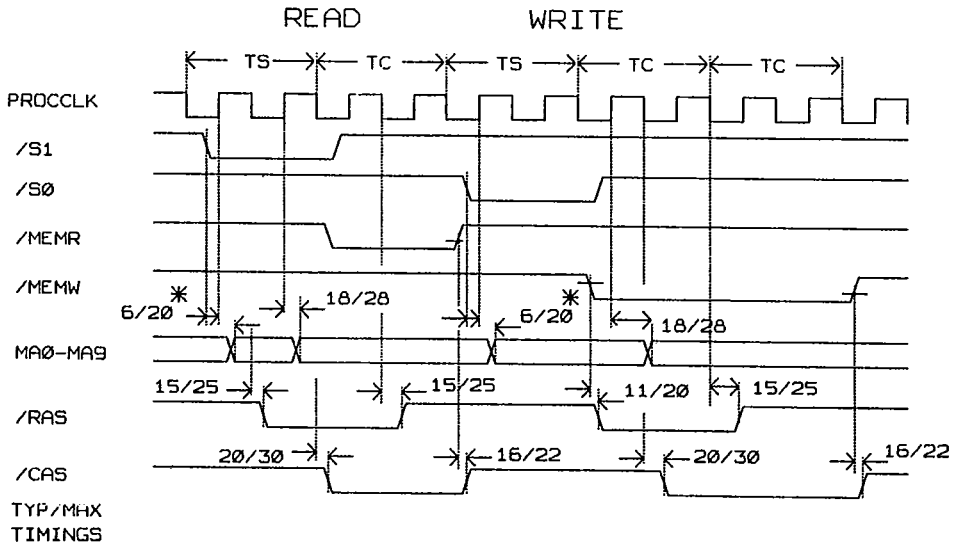


IOCHRDY =1
/0WS =1
ROMSEL =1

* NOTE: TYP/MAX TIMINGS
RELATIVE TO LATER OF 2 EDGES
(PROCCLK RISING or S0*/S1*)

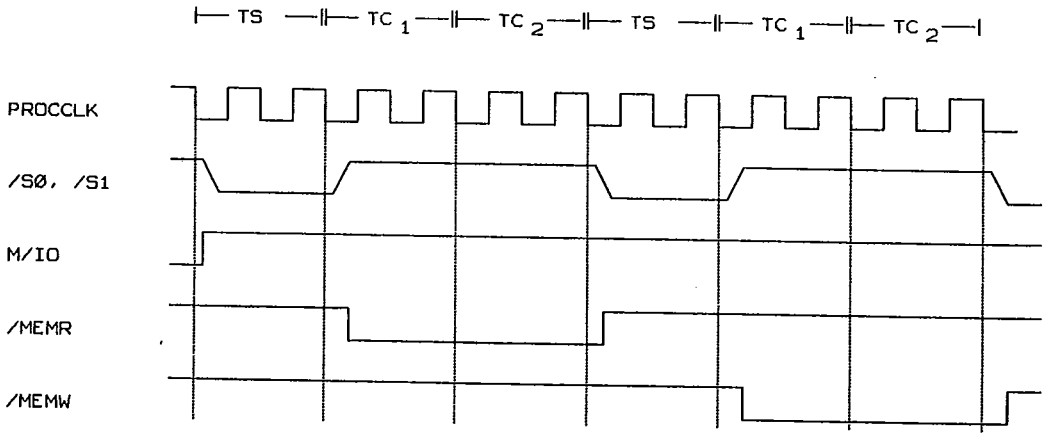
INTERNAL DELAY TIMING

286 Mode



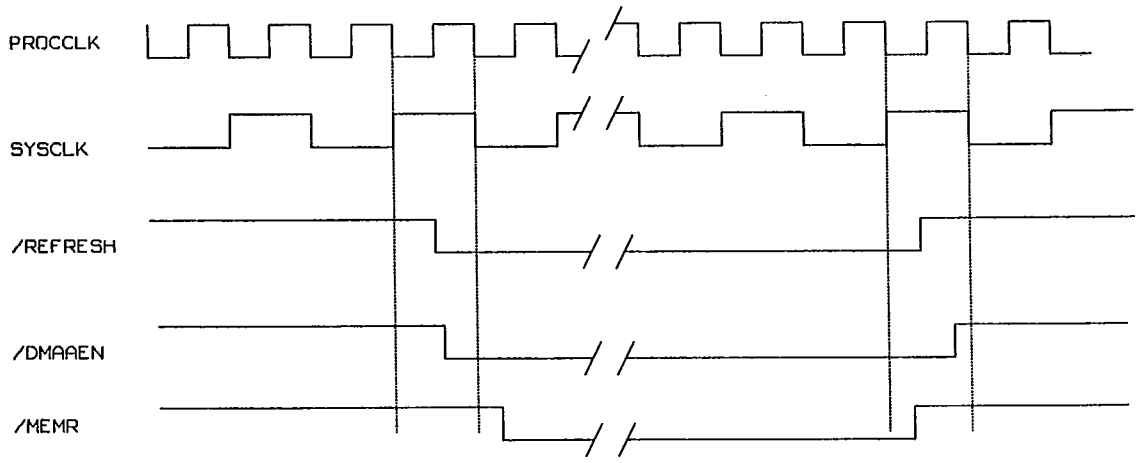
READ THEN WRITE, MEMORY CYCLE

286 Mode



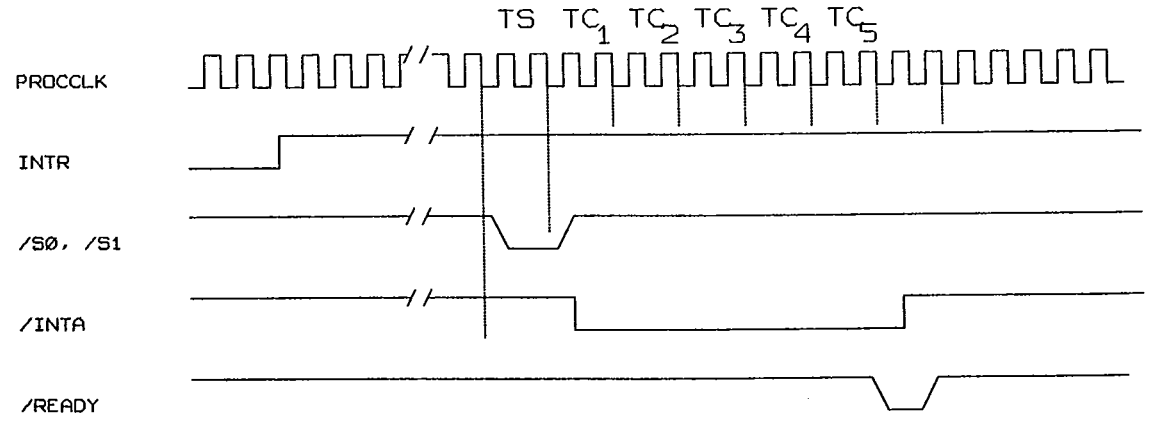
REFRESH TIMING

286 Mode



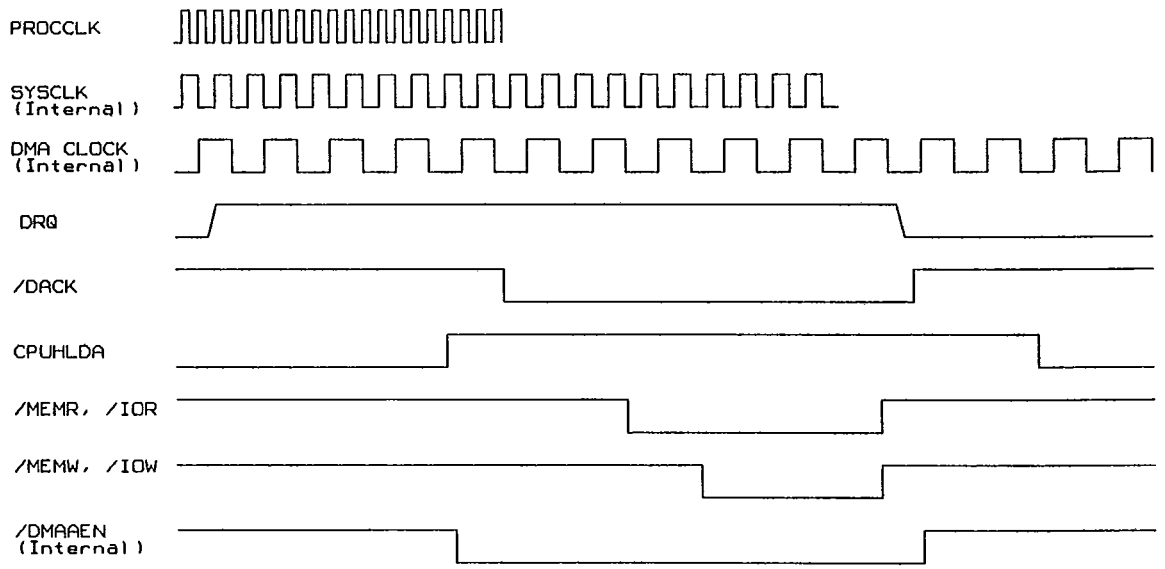
INTERRUPT TIMING

286 Mode



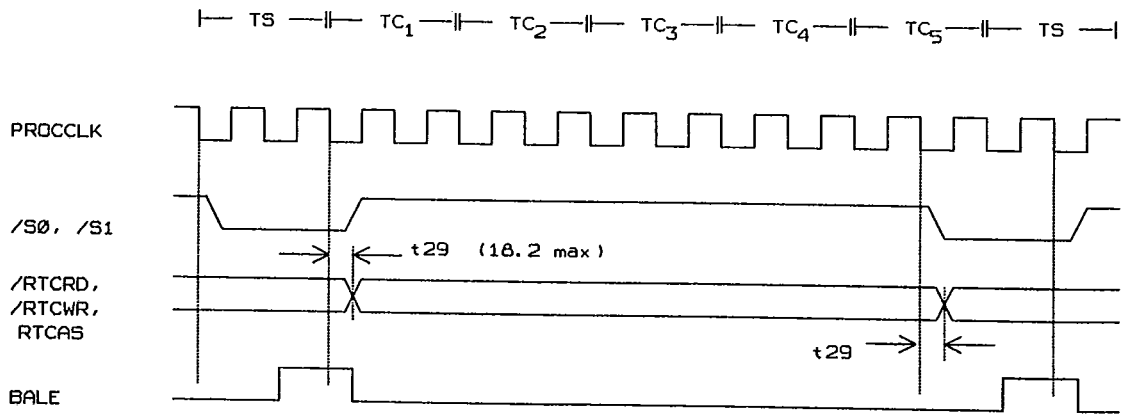
DMA ACKNOWLEDGE

286 Mode



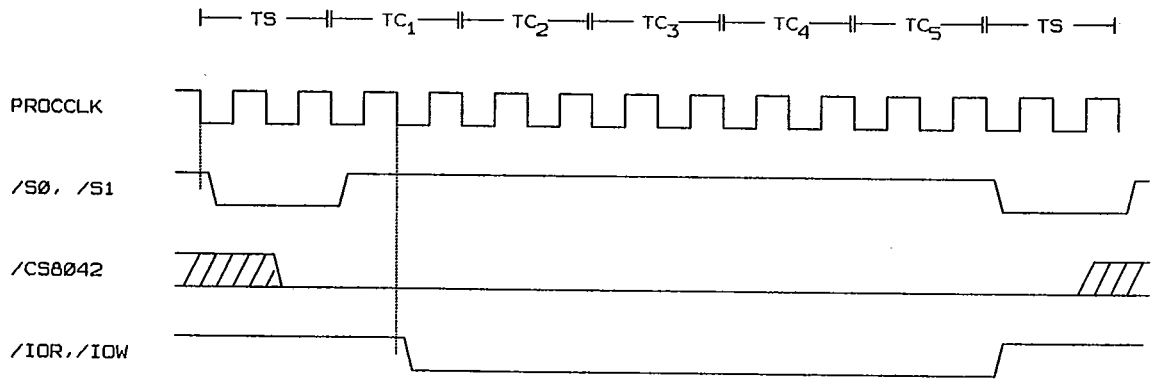
REAL TIME CLOCK ACCESS

286 Mode



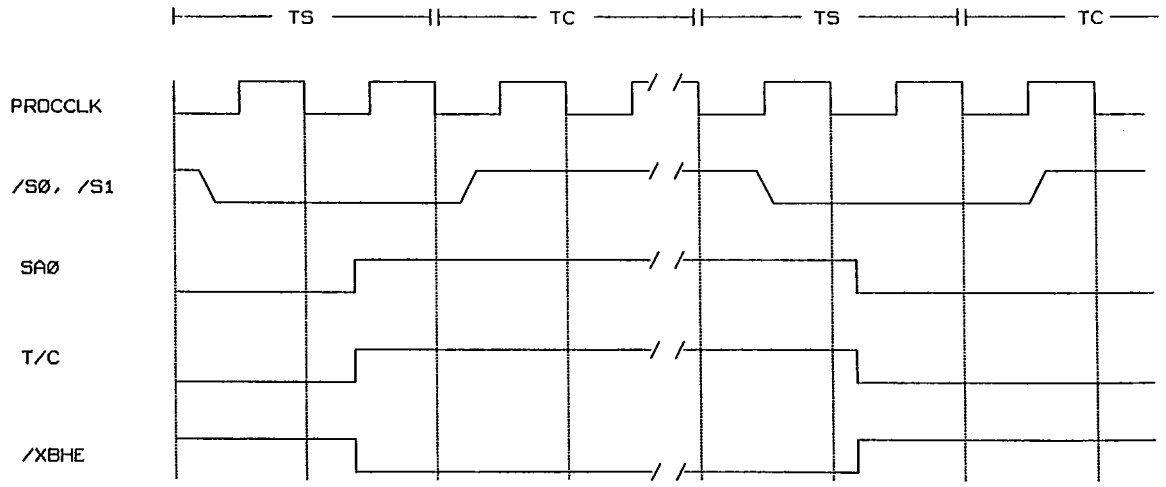
KEYBOARD CONTROLLER I/O TIMING

286 Mode

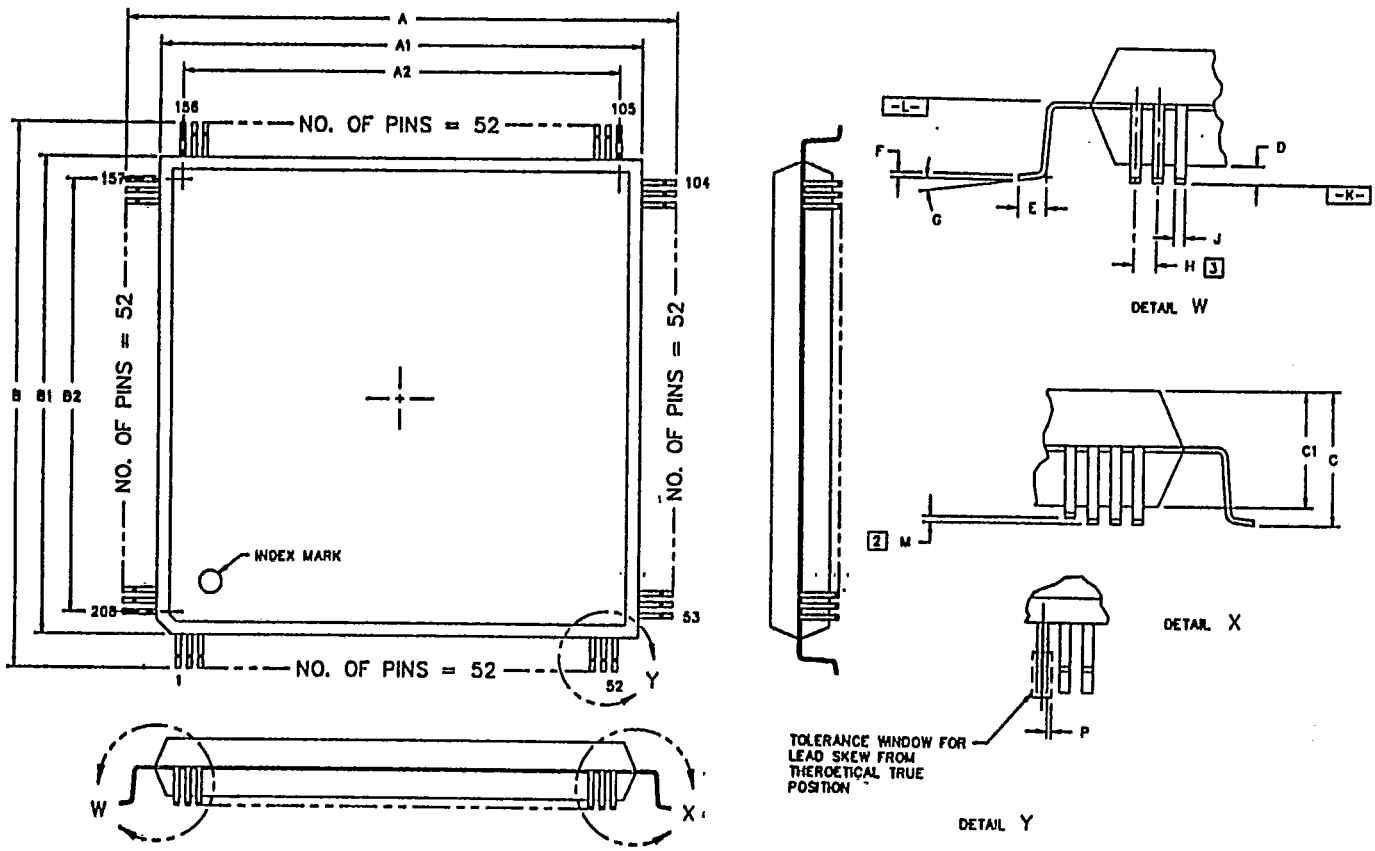


SAO, TC AND /XBHE TIMING

286 Mode



HT21
208 Pin Plastic Flat Pack



IMPORTANT NOTE:

If designing in inches, ALL pin positions should be calculated in millimeters (mm) then converted to inches. The inches listed have been rounded.

SYM	DIMENSIONS IN MM MINIMUM	MAXIMUM
A	30.30	31.50
A1	27.90	28.10
A2	25.50 REF	
B	30.30	31.50
B1	27.90	28.10
B2	25.50 REF	
C	3.68	4.01
C1	3.43	3.66
D	0.25	0.36
E	0.60	1.00
F	0.10	0.25
G	0°	10°
H	0.40	0.60
J	0.15	0.25
M	0.10 Max	
P	0.05 Max	
Total No. of Pins	208	

SYM	DIMENSIONS IN INCHES MINIMUM	MAXIMUM
A	1.193	1.240
A1	1.098	1.106
A2	1.004 REF	
B	1.193	1.240
B1	1.098	1.106
B2	1.004 REF	
C	.145	.158
C1	.135	.144
D	.010	.014
E	.024	.039
F	.004	.010
G	0°	10°
H	.020+/-.004	
J	.006	.010
M	.004 Max	
P	.002 Max	
Total No. of Pins	208	

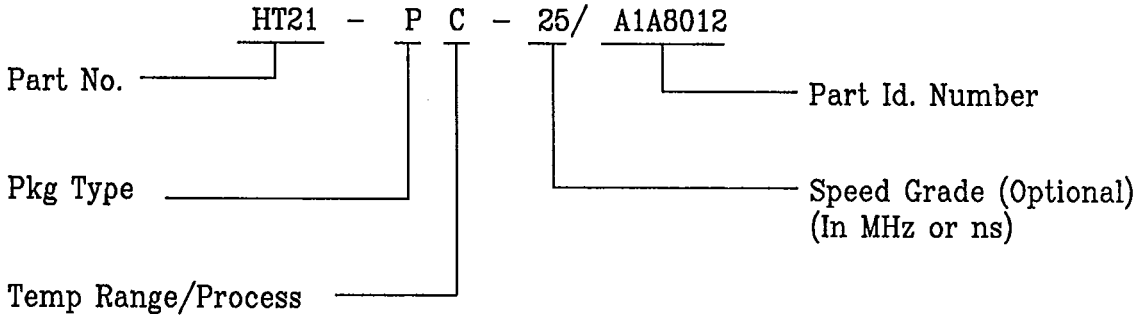
NOTES:

1. Coplaniarity of all leads shall be within 0.1MM (0.004") (Difference between highest and lowest lead with seating plane -K- as reference)

2. Lead pitch determined at datum -L-.

Product Ordering Information & Part Marking

Order Code/Part Number Example



Temp Range/Process

C – Commercial temp range (0°C to 70°C)
I – Industrial temp range (–40°C to +85°C)

Package Types

P – Plastic

IMPORTANT: Contact your local sales office for the current Order Code/Part Number