CL-GD5480

Advance Data Book

FEATURES

- **64-bit high-bandwidth synchronous DRAM interface**
  - — 800 Mbytes/sec. peak memory bandwidth
  - — Supports modes up to 1600 × 1200, 64K colors at 60 Hz and 1280 × 1024, 16.8M colors at 75 Hz
  - — Provides significant additional memory bandwidth for BitBLT (bit boundary block transfer) and video window operations, even in high-resolution/color-depth graphics and video modes
- **Microsoft® PC97-compliant**
  - — Direct access to frame buffer independent of BitBLT
  - — Relocated VGA and BitBLT registers
  - — System, subsystem vendor ID
  - — Low-resolution modes for Direct3D™
- **Video conferencing advantages**
  - — Glueless digital camera interface with direct support of CCIR (ITR-U, International Radio Consultive Committee) 6:5:6 format
  - — Dual-hardware video window for local and remote viewing
  - — Optional PCI bus master conversion to YUV 4:2:0 for off-loading CPU during local view transmission
  - — Remote and local view mirror image and vertical flip options
  - — Continuous XY filtered downscaling for video conference display size
- **Intel® Intercast™ support**
  - — Luminance-only video capture mode for efficient VBI (vertical blanking interval) data processing
  - — Simultaneous capture and transfer of VBI data to system memory while TV picture is displayed in the video window
  - — PCI bus master write operation for fast transfer of VBI data to system memory without CPU intervention
- **MPEG playback assist**
  - — Playback support for native MPEG format of planar YUV 4:2:0, freeing CPU of conversion burden
- **3 × 8 palette LUT with independent RGB addressing for color adjustment (such as gamma correction) in 15-, 16-, and 24-bpp modes**

64-Bit SGRAM GUI Accelerator

OVERVIEW

The CL-GD5480 is the latest member of the Cirrus Logic Alpine™ family and interfaces to a high-speed SGRAM (synchronous graphics RAM) frame buffer. This device delivers a high-performance combination of graphics, animation, better-than-TV quality full-screen video, and software 3D acceleration in an integrated single-chip device.

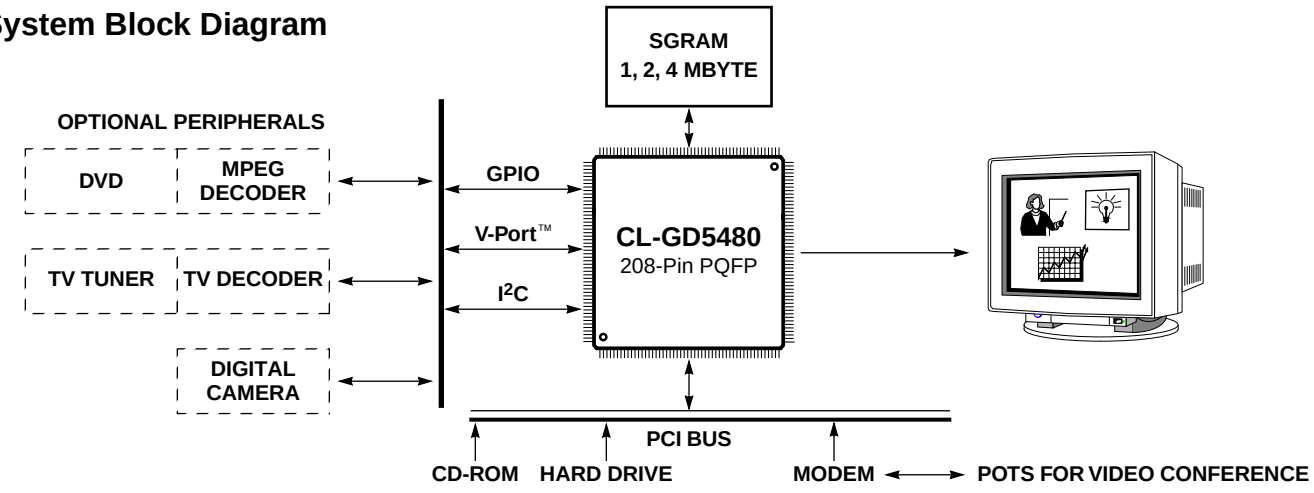
Packaged in a 208-pin PQFP and using the industry-standard V-Port™ to interface directly to various video input devices, the CL-GD5480 offers a highly cost-effective and flexible VisualMedia™ solution.

The V-Port, GPIO, and I^2C bus interfaces provide a glueless connection to external devices to play back disk-based video files (including MPEG), and to provide TV-in-a-window, closed captioning, Intercast™, and video conferencing.

The CL-GD5480 has many features designed specifically to optimize Microsoft® DirectDraw™ performance. Hardware support for Microsoft Direct3D™ software also enables a cost-effective 3D visual system.

The CL-GD5480 is software-compatible with the Cirrus Logic Alpine™ family, featuring the industry's most stable software drivers, most extensive software QA process, and best language localization support. The VPM™ (video port manager) interface, an industry-standard driver API created by Cirrus Logic for Windows® 3.1x and Windows® 95, provides an easy path for V-Port peripheral application software development.

System Block Diagram



ADVANTAGES	BENEFITS
Outstanding VisualMedia™ Acceleration	
■ BitBLT command list in off-screen memory	❒ Enhances graphics performance, especially for text.
■ 100-MHz synchronous memory (SGRAM) interface	❒ Faster screen refresh performance for higher resolutions and monitor refresh rate support.
■ PCI bus master writes of captured video data streams	❒ Increases performance of video capture-to-system memory transfers for multiple applications, such as video conferencing, Intercast™, and software 3D acceleration.
■ High-performance PCI bus interface	❒ Provides ample interface speed margin compared with available and next-generation core logic chipsets.
■ Full PCI v2.1-compliance	❒ Interfaces easily to high-performance core logic chipsets.
■ Vertical scanline readback, display double-buffering support, and transparent BitBLT operations	❒ Optimizes display page-flipping support for outstanding games animation performance under DirectDraw™.
■ Z,C interleave data separation on system-to-screen write	❒ Accelerates software 3D performance.
Superior Video Performance	
■ Advanced video playback features with continuous interpolated zoom/shrink, and color/chroma key overlay for all modes	❒ Maintains high-quality video over a wide range of sizing options with video and graphics overlay support in all color depths.
■ YUV 4:2:0 display support including 4:2:2-to-4:2:0 capture conversion option	❒ Accelerates MPEG-2 native codec playback and capture.
■ Second hardware video window support	❒ Allows display of video conferencing local view.
■ Patented multiformat frame buffer with independent memory apertures for BitBLT and CPU/video operations	❒ Allows concurrent operations and independent graphics/video color depths for efficient memory/bandwidth usage.
Cost-Effective Design and Integration	
■ Advanced 0.4-µm CMOS process	❒ Higher speed and performance margin with low-power operation.
■ Cirrus Logic–owned manufacturing capacity	❒ Full control and access to advanced manufacturing processes.
■ Video capture V-Port™ interface to external video devices	❒ Eliminates the need for a separate video frame buffer, lowering overall system cost.
■ GPIO and I^2C interfaces	❒ Provides a low-cost control interface for applications such as TV tuners, DVD (digital video disk) drives, and digital cameras.
■ Integrated dual synthesizer and filters, oscillator, 200-MHz RAMDAC and current reference	❒ Lower overall system implementation cost.
Compatibility and Ease of System Design	
■ Industry's best VisualMedia™ software support	❒ Extensive QA process and maintenance program ensures high quality and maximum customer satisfaction.
■ Compatible with CL-GD5446 software	❒ Based on production-proven, high-quality software.
■ Localization support	❒ Complete utility localization for 21 languages.
■ Cirrus Logic TVTap™ application software	❒ TV decoder software for CL-GD5480 interface with the most popular video decoders and tuners.
■ VPM™ provider for Windows® 3.1x and Windows® 95	❒ Eases peripheral-application software development.
■ VMI 1.4-compatible	❒ Easy connection to external video devices.
■ Supports ×32 SGRAMs up to 100 MHz	❒ Allows multiple memory configurations and vendors.
■ Compatible with VGA and VESA® standards	❒ Compatible with installed base of systems and software.

SOFTWARE SUPPORT

DRIVERS

- **Microsoft® Windows® 95**
- **Microsoft® Windows® NT™ v3.51, v4.0**
- **Microsoft® Windows® 3.1x**
- **OS/2® v2.1, v2.11, v3.0**
- **AutoCAD® v12.0, v13.0**
- **MicroStation**
- **UNIX® (Solaris, SCO, Unixware)**
- **VPM provider under Windows® 3.1x and Windows® 95**

BIOS SUPPORT

- **IBM® VGA-compatible BIOS**
- **32 Kbytes with PCI bus support**
- **Adapter or motherboard implementation**
- **VBE™ 2.0 (VESA® BIOS extensions) support in ROM**
- **Support for DPMS (display power management signaling) in ROM**
- **VESA® monitor timing-compliant**
- **DDC2B support**

UTILITIES

- **Graphics and video diagnostics test**
- **Windows® NT™ and DOS utilities**
- **Display mode configuration utility — CLMODE**
- **Set resolution in Windows® utility — WINMODE**
- **Configurable system integration for OEMs — OEMSI**
- **DMI (desktop management interface) support**
- **Gamma correction user interface**
- **EZREZ: Windows® 3.1 resolution/color depth change on-the-fly**
- **Windows® 95 refresh rate/resolution/color depth change utility**

LOCALIZATION

- **Simplified Chinese**
- **Traditional Chinese**
- **Czech**
- **Danish**
- **Dutch**
- **Finnish**
- **French**
- **German**
- **Hungarian**
- **Italian**
- **Japanese**
- **Korean**
- **Norwegian**
- **Polish**
- **Brazilian Portuguese**
- **Portuguese**
- **Russian**
- **Latin American Spanish**
- **Spanish**
- **Swedish**
- **Thai**

CL-GD5480 Extended Display Modes and Refresh Rates (Hz)

Resolution	16 Colors	256 Colors	32K/64K Colors	16.8M Colors
640 × 400	–	70	–	–
640 × 480	60 (standard VGA)	60, 72, 75, 85, 100		
800 × 600	56, 60, 72, 75	56, 60, 72, 75, 85, 100		
1024 × 768	43i[a], 60, 70, 75	43i, 60, 70, 75, 85, 100		43i, 60, 70, 75, 85
1152 × 864	–	70, 75, 85, 100	70, 75, 85	70, 75
1280 × 1024	43i	43i, 60, 75, 85		43i, 60
1600 × 1200	–	48i, 60		–

[a] 'i' indicates interlaced.

APPLICATIONS SUPPORT

- **Technical reference manual and design kit — complete data book, electrical specifications, register set definitions, pin descriptions, reference designs, and applications information.**
- **BIOS and driver release kits — contains user guides, PDR (problem description report) forms, source code license agreement, and quality assurance procedures.**
- **PCI board evaluation kit — adapter card including CL-GD5480, on-board BIOS, and 2-Mbyte SGRAM shipped with complete design package (schematics, Gerber® files) and software drivers.**
- **Electronic information services:**
  - — ftp: ftp.cirrus.com
  - — World Wide Web: http://www.cirrus.com
  - — BBS: (510) 440-9080
  - — Fax-on-demand: (510) 249-4200

Table of Contents

CONVENTIONS

Abbreviations

Symbol	Units of measure
°C	degree Celsius
Hz	hertz (cycles per second)
Kbyte	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbyte	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
µF	microfarad
µs	microsecond (1,000 nanoseconds)
mA	milliampere
ms	millisecond (1,000 microseconds)
ns	nanosecond
pV	picovolt

The use of 'tbd' indicates values that are 'to be determined', 'n/a' designates 'not available', and 'n/c' indicates a pin that is a 'no connect'.

Acronyms

Acronym	Definition
AC	alternating current
ALU	arithmetic logic unit
ATE	automatic test equipment
BIOS	basic input/output system
BitBLT, BLT	bit boundary block transfer
bpp	bits per pixel
CAD	computer-aided design
CAS	column address strobe
CGA	color graphics adapter
CLUT	color lookup table
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
CRT	cathode ray tube
CRTC	CRT controller

Acronym	Definition
DAC	digital-to-analog converter
DC	direct current
DDA	digital differential algorithm
DDC	display data channel
DMI	desktop management signaling
DPMS	display power management signaling
DRAM	dynamic random access memory
dword	doubleword (16 bytes)
EEPROM	electrically erasable/programmable read-only memory
EGA	enhanced graphics adapter
EPROM	electrically programmable read-only memory
EVAFC	extended VESA® advanced feature connector

Acronym	Definition
FIFO	first in/first out
GPIO	general-purpose IO
GSC	graphics system controller
GUI	graphical user interface
HDR	Hidden DAC register
HRQ	host read queue
HSYNC/VSYNC	horizontal/vertical synchronization
HWQ	host write queue
IC	integrated circuit
I/O	input/output
LBI	local bus interface
LSB	least-significant bit
LUT	lookup table
MA	memory arbiter
MC	memory controller
MCC	monochrome-to-color converter
MD	memory data
MMI/O	memory-mapped I/O
MSB	most-significant bit
OFU	operand fetch unit
OSU	operand storage unit
PCI	peripheral component interconnect
PFS	programmable frequency synthesizer
PLL	phase-locked loop
PQFP	plastic quad-flat pack

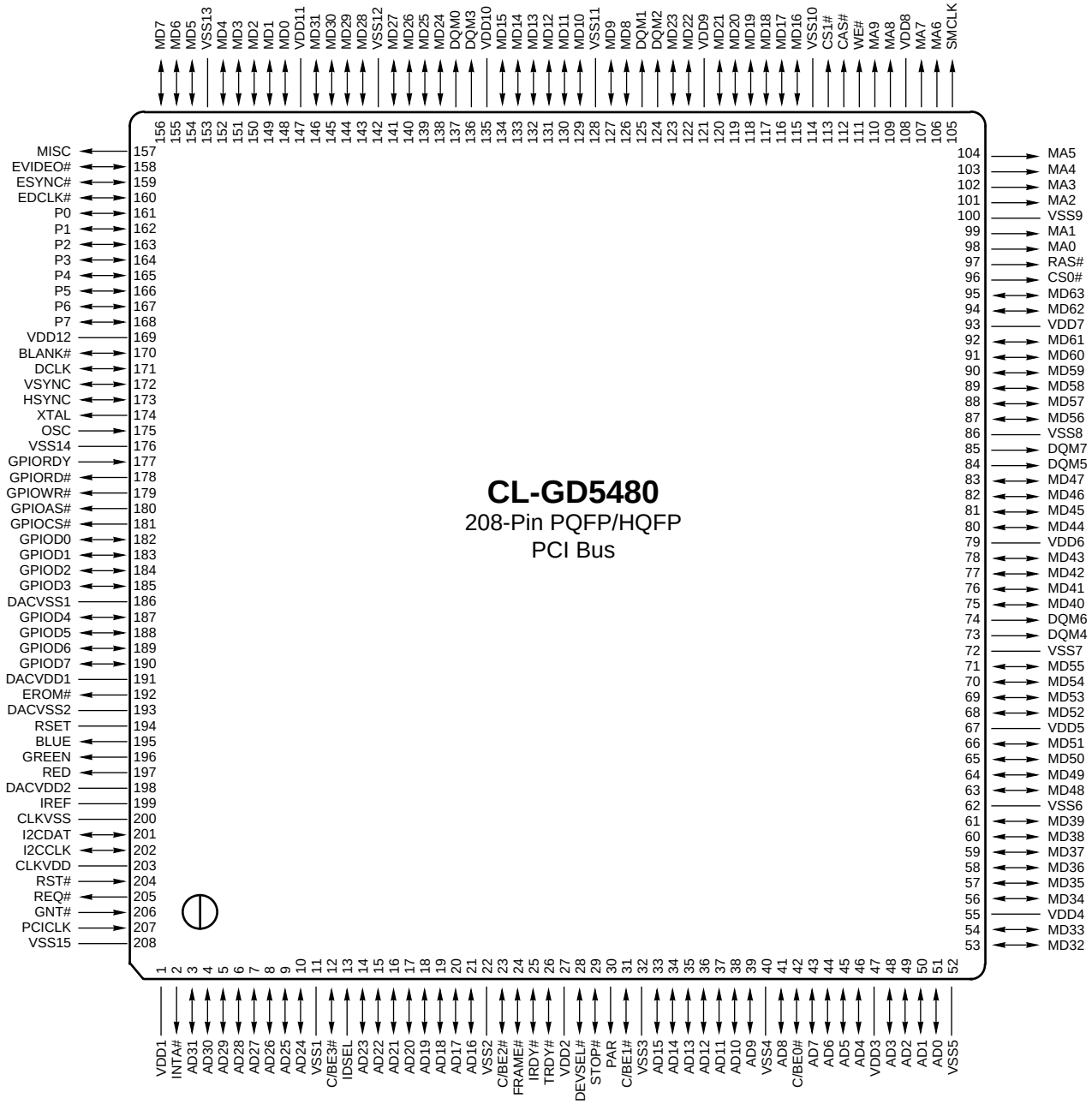
Acronym	Definition
qword	two dwords
RAC	Rambus® access channel
RAM	random-access memory
RAS	row address strobe
RDRAM	Rambus® dynamic random-access memory
RGB	red, green, and blue
RIF	Rambus® interface
ROPs	raster operations
RSU	result storage unit
R/W	read/write
SC	serial clock
SG	signature generator
SGRAM	synchronous graphics RAM
SRAM	static random-access memory
TSR	terminate and stay resident
TTL	transistor-transistor logic
VBE	VESA BIOS extensions
VBI	vertical blanking interval
VDD	virtual device driver
VESA®	Video Electronics Standards Association
VGA	video graphics array
VL	VESA® local
VPM	video port manager
VRAM	video random-access memory
WE	write enable

Numeric Naming

Hexadecimal numbers are represented with all letters in upper case and a lower-case ‘h’ is appended to them (for example, ‘14h’, ‘3A7h’, and ‘C000h’ are hexadecimal numbers). Binary numbers are represented with a lower-case ‘b’ appended. Numbers not indicated by a ‘b’ or an ‘h’ are decimal.

1. PIN INFORMATION

The CL-GD5480 is available in a 208-pin PQFP (plastic quad flat pack) or HQFP (high-performance quad flat pack) for the PCI bus only.



1.1 Pin Summary

Many of the pins on the CL-GD5480 are multi-purpose and pin types vary according to function. Each multi-purpose pin appears in two or more of the following tables. In each table, the pin type and loading information reflect the use described in that table. The following abbreviations are used for pin types in the following tables: (I) indicates input; (O) indicates output; (O-Z) indicates tristate output; (OC) indicates open-collector output; (BIO) indicates bidirectional I/O.

Table 1-1. Host Interface

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
IDSEL	13	I				
RST#	204	I				
PCICLK	207	I				
GNT#	206	I				
FRAME#	24	BIO		–3	8	240
IRDY#	25	BIO		–3	8	240
TRDY#	26	BIO		–3	8	240
DEVSEL#	28	BIO		–3	4	200
STOP#	29	BIO		–3	8	240
PAR	30	O		–3	8	240
REQ#	205	O		–3	8	240
INTA#	2	OC		(OC)	8	240
C/BE#3	12	BIO		–3	8	240
C/BE#2	23	BIO		–3	8	240
C/BE#1	31	BIO		–3	8	240
C/BE#0	42	BIO		–3	8	240
AD31	3	BIO		–3	12	240
AD30	4	BIO		–3	12	240
AD29	5	BIO		–3	12	240
AD28	6	BIO		–3	12	240
AD27	7	BIO		–3	12	240
AD26	8	BIO		–3	12	240
AD25	9	BIO		–3	12	240
AD24	10	BIO		–3	12	240
AD23	14	BIO		–3	12	240

Table 1-1. Host Interface *(cont.)*

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
AD22	15	BIO		–3	12	240
AD21	16	BIO		–3	12	240
AD20	17	BIO		–3	12	240
AD19	18	BIO		–3	12	240
AD18	19	BIO		–3	12	240
AD17	20	BIO		–3	12	240
AD16	21	BIO		–3	12	240
AD15	33	BIO		–3	12	240
AD14	34	BIO		–3	12	240
AD13	35	BIO		–3	12	240
AD12	36	BIO		–3	12	240
AD11	37	BIO		–3	12	240
AD10	38	BIO		–3	12	240
AD9	39	BIO		–3	12	240
AD8	41	BIO		–3	12	240
AD7	43	BIO		–3	12	240
AD6	44	BIO		–3	12	240
AD5	45	BIO		–3	12	240
AD4	46	BIO		–3	12	240
AD3	48	BIO		–3	12	240
AD2	49	BIO		–3	12	240
AD1	50	BIO		–3	12	240
AD0	51	BIO		–3	12	240

[a] Indicates nominal 250-kΩ pull-up resistor.

Table 1-2. BIOS ROM

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Also Used As:
BIOSA14	158	O	●	–3	8	50	EVIDEO# (I), VACT (I)
BIOSA13	159	O	●	–3	8	50	ESYNC# (I)
BIOSA12	160	O	●	–3	8	50	EDCLK# (I), VREF (I)
BIOSA11	180	O		–3	8	50	GPIOAS# (O)
BIOSA10	178	O		–3	8	50	GPIORD# (O)
BIOSA9	179	O		–3	8	50	GPIOWR# (O)
BIOSA8	170	O		–3	8	50	BLANK# (BIO), HREF (I)
BIOSA7	168	O		–3	8	50	P7 (BIO), PIXD7 (I)
BIOSA6	167	O		–3	8	50	P6 (BIO), PIXD6 (I)
BIOSA5	166	O		–3	8	50	P5 (BIO), PIXD5 (I)
BIOSA4	165	O		–3	8	50	P4 (BIO), PIXD4 (I)
BIOSA3	164	O		–3	8	50	P3 (BIO), PIXD3 (I)
BIOSA2	163	O		–3	8	50	P2 (BIO), PIXD2 (I)
BIOSA1	162	O		–3	8	50	P1 (BIO), PIXD1 (I)
BIOSA0	161	O		–3	8	50	P0 (BIO), PIXD0 (I)
BIOSD7	190	I					GPIOD7 (BIO), OUT1 (O)
BIOSD6	189	I	●				GPIOD6 (BIO), OUT0, CF7
BIOSD5	188	I	●				GPIOD5 (BIO), CF6
BIOSD4	187	I	●				GPIOD4 (BIO), GPIOA4 (O), CF5
BIOSD3	185	I	●				GPIOD3 (BIO), GPIOA3 (O), CF4
BIOSD2	184	I	●				GPIOD2 (BIO), GPIOA2 (O), CF3
BIOSD1	183	I	●				GPIOD1 (BIO), GPIOA1 (O), CF2
BIOSD0	182	I	●				GPIOD0 (BIO), GPIOA0 (O), CF1, IN0
EROM#	192	O		–12	12	35	

[a] Indicates nominal 250-kΩ pull-up resistor.

Table 1-3. Display Memory Interface

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
SMCLK	105	O		–12	12	50
RAS#	97	O		–12	12	50
CAS#	112	O		–12	12	50
CS0#	96	O		–12	12	50
CS1#	113	O		–12	12	50
WE#	111	O		–12	12	50
DQM7	85	O		–12	12	50
DQM6	74	O		–12	12	50
DQM5	84	O		–12	12	50
DQM4	73	O		–12	12	50
DQM3	136	O		–12	12	50
DQM2	124	O		–12	12	50
DQM1	125	O		–12	12	50
DQM0	137	O		–12	12	50
MA9	110	O		–12	12	150
MA8	109	O		–12	12	150
MA7	107	O		–12	12	150
MA6	106	O		–12	12	150
MA5	104	O		–12	12	150
MA4	103	O		–12	12	150
MA3	102	O		–12	12	150
MA2	101	O		–12	12	150
MA1	99	O		–12	12	150
MA0	98	O		–12	12	150
MD63	95	BIO	●	–8	8	50
MD62	94	BIO	●	–8	8	50
MD61	92	BIO	●	–8	8	50
MD60	91	BIO	●	–8	8	50
MD59	90	BIO	●	–8	8	50
MD58	89	BIO	●	–8	8	50

Table 1-3. Display Memory Interface *(cont.)*

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
MD57	88	BIO	●	–8	8	50
MD56	87	BIO	●	–8	8	50
MD55	71	BIO	●	–8	8	50
MD54	70	BIO	●	–8	8	50
MD53	69	BIO	●	–8	8	50
MD52	68	BIO	●	–8	8	50
MD51	66	BIO	●	–8	8	50
MD50	65	BIO	●	–8	8	50
MD49	64	BIO	●	–8	8	50
MD48	63	BIO	●	–8	8	50
MD47	83	BIO	●	–8	8	50
MD46	82	BIO	●	–8	8	50
MD45	81	BIO	●	–8	8	50
MD44	80	BIO	●	–8	8	50
MD43	78	BIO	●	–8	8	50
MD42	77	BIO	●	–8	8	50
MD41	76	BIO	●	–8	8	50
MD40	75	BIO	●	–8	8	50
MD39	61	BIO	●	–8	8	50
MD38	60	BIO	●	–8	8	50
MD37	59	BIO	●	–8	8	50
MD36	58	BIO	●	–8	8	50
MD35	57	BIO	●	–8	8	50
MD34	56	BIO	●	–8	8	50
MD33	54	BIO	●	–8	8	50
MD32	53	BIO	●	–8	8	50
MD31	146	BIO	●	–8	8	50
MD30	145	BIO	●	–8	8	50
MD29	144	BIO	●	–8	8	50
MD28	143	BIO	●	–8	8	50

Table 1-3. Display Memory Interface *(cont.)*

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
MD27	141	BIO	●	–8	8	50
MD26	140	BIO	●	–8	8	50
MD25	139	BIO	●	–8	8	50
MD24	138	BIO	●	–8	8	50
MD23	123	BIO	●	–8	8	50
MD22	122	BIO	●	–8	8	50
MD21	120	BIO	●	–8	8	50
MD20	119	BIO	●	–8	8	50
MD19	118	BIO	●	–8	8	50
MD18	117	BIO	●	–8	8	50
MD17	116	BIO	●	–8	8	50
MD16	115	BIO	●	–8	8	50
MD15	134	BIO	●	–8	8	50
MD14	133	BIO	●	–8	8	50
MD13	132	BIO	●	–8	8	50
MD12	131	BIO	●	–8	8	50
MD11	130	BIO	●	–8	8	50
MD10	129	BIO	●	–8	8	50
MD9	127	BIO	●	–8	8	50
MD8	126	BIO	●	–8	8	50
MD7	156	BIO	●	–8	8	50
MD6	155	BIO	●	–8	8	50
MD5	154	BIO	●	–8	8	50
MD4	152	BIO	●	–8	8	50
MD3	151	BIO	●	–8	8	50
MD2	150	BIO	●	–8	8	50
MD1	149	BIO	●	–8	8	50
MD0	148	BIO	●	–8	8	50

[a] ● indicates the presence of an internal 250-kΩ ± 50% pull-up resistor.

Table 1-4. Monitor Interface

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
VSYNC	172	BIO		–12	24	50
HSYNC	173	BIO		–12	24	50
RED	197	Analog Out				
GREEN	196	Analog Out				
BLUE	195	Analog Out				
IREF	199	Analog				
RSET	194	Analog				

[a] ● indicates the presence of an internal 250-kΩ ± 50% pull-up resistor.

Table 1-5. Pass-Through Connector

Pin Name	Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Also Used As:
BLANK#	170	BIO		–12	12	50	BIOSA8 (O), HREF (I)
P7	168	BIO		–12	12	50	BIOSA7 (O), PIXD7 (I)
P6	167	BIO		–12	12	50	BIOSA6 (O), PIXD6 (I)
P5	166	BIO		–12	12	50	BIOSA5 (O), PIXD5 (I)
P4	165	BIO		–12	12	50	BIOSA4 (O), PIXD4 (I)
P3	164	BIO		–12	12	50	BIOSA3 (O), PIXD3 (I)
P2	163	BIO		–12	12	50	BIOSA2 (O), PIXD2 (I)
P1	162	BIO		–12	12	50	BIOSA1 (O), PIXD1 (I)
P0	161	BIO		–12	12	50	BIOSA0 (O), PIXD0 (I)
DCLK	171	BIO		–12	12	50	PIXCLK (I)
EVIDEO#	158	I	●				BIOSA14 (O), VACT (I)
ESYNC#	159	I	●				BIOSA13 (O)
EDCLK#	160	I	●				BIOSA12 (O), VREF (I)

[a] ● indicates the presence of an internal 250-kΩ ±50% pull-up resistor.

Table 1-6. General-Purpose I/O

Pin Name	Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Also Used As:
GPIOD7	190	BIO	–3	8	50	BIOSD7 (I), OUT1 (O)
GPIOD6	189	BIO	–3	8	50	BIOSD6 (I), OUT0 (O), CF7
GPIOD5	188	BIO	–3	8	50	BIOSD5 (I), CF6
GPIOD4	187	BIO	–3	8	50	BIOSD4 (I), GPIOA4 (O), CF5
GPIOD3	185	BIO	–3	8	50	BIOSD3 (I), GPIOA3 (O), CF4
GPIOD2	184	BIO	–3	8	50	BIOSD2 (I), GPIOA2 (O), CF3
GPIOD1	183	BIO	–3	8	50	BIOSD1 (I), GPIOA1 (O), CF2
GPIOD0	182	BIO	–3	8	50	BIOSD0 (O), GPIOA0 (O), CF1, IN0 (I)
GPIOCS#	181	O	–3	8	50	
GPIOAS#	180	O	–3	8	50	BIOSA11 (O)
GPIOWR#	179	O	–3	8	50	BIOSA9 (O), GPIODS#(O)
GPIORD#	178	O	–3	8	50	BIOSA10 (O), GPIOR/W# (O)
GPIORDY	177	I				GPIODTACK# (I)

Table 1-7. V-Port™

Pin Name	Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Also Used As:
HREF	170	I				BIOSA8 (O), BLANK# (BIO)
VREF	160	I				BIOSA12 (O), EDCLK# (I)
VACT	158	I				BIOSA14 (O), EVIDEO# (I)
PIXCLK	171	I				DCLK (BIO)
PIXD7	168	I				BIOSA7 (O), P7 (BIO)
PIXD6	167	I				BIOSA6 (O), P6 (BIO)
PIXD5	166	I				BIOSA5 (O), P5 (BIO)
PIXD4	165	I				BIOSA4 (O), P4 (BIO)
PIXD3	164	I				BIOSA3 (O), P3 (BIO)
PIXD2	163	I				BIOSA2 (O), P2 (BIO)
PIXD1	162	I				BIOSA1 (O), P1 (BIO)
PIXD0	161	I				BIOSA0 (O), P0 (BIO)

Table 1-8. Miscellaneous Pins

Pin Name	Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Also Used As:
OSC	175	I				
XTAL	174	Analog				
I2CDAT	201	BIO	(OC)	12	35	
I2CCLK	202	BIO	(OC)	12	35	
MISC	157	O-Z	–3	8		Color Key, BLT Busy

Table 1-9. Power[a] and Ground

Pin Name	Pin Number	Connection	Note
VDD1	1	Power	Digital
VDD2	27	Power	Digital
VDD3	47	Power	Digital
VDD4	55	Power	Digital
VDD5	67	Power	Digital
VDD6	79	Power	Digital
VDD7	93	Power	Digital
VDD8	108	Power	Digital
VDD9	121	Power	Digital
VDD10	135	Power	Digital
VDD11	147	Power	Digital
VDD12	169	Power	Digital
VSS1	11	Ground	Digital
VSS2	22	Ground	Digital
VSS3	32	Ground	Digital
VSS4	40	Ground	Digital
VSS5	52	Ground	Digital
VSS6	62	Ground	Digital
VSS7	72	Ground	Digital
VSS8	86	Ground	Digital

Table 1-9. Power[a] and Ground *(cont.)*

Pin Name	Pin Number	Connection	Note
VSS9	100	Ground	Digital
VSS10	114	Ground	Digital
VSS11	128	Ground	Digital
VSS12	142	Ground	Digital
VSS13	153	Ground	Digital
VSS14	176	Ground	Digital
VSS15	208	Ground	Digital
DACVDD1	191	DAC Power	DAC
DACVDD2	198	DAC Power	DAC
DACVSS1	186	DAC Ground	DAC
DACVSS2	193	DAC Ground	DAC
CLKVDD	203	Isolated Power	Synthesizers
CLKVSS	200	Isolated Ground	Synthesizers

[a] Nominal VDD is 3.3 V.

Table 1-10. Pins with Multiple Uses (Ordered by Pin Number)

Pin Number	BIOS ROM	Pass-through Connector	V-Port™	GPIO	Other	Pin Diagram
158	BIOSA14 (O)	EVIDEO# (I)	VACT (I)	–	–	I/O
159	BIOSA13 (O)	ESYNC# (I)	–	–	–	I/O
160	BIOSA12 (O)	EDCLK# (I)	VREF (I)	–	–	I/O
161	BIOSA0 (O)	PO (BIO)	PIXD0 (I)	–	–	I/O
162	BIOSA1 (O)	P1 (BIO)	PIXD1 (I)	–	–	I/O
163	BIOSA2 (O)	P2 (BIO)	PIXD2 (I)	–	–	I/O
164	BIOSA3 (O)	P3 (BIO)	PIXD3 (I)	–	–	I/O
165	BIOSA4 (O)	P4 (BIO)	PIXD4 (I)	–	–	I/O
166	BIOSA5 (O)	P5 (BIO)	PIXD5 (I)	–	–	I/O
167	BIOSA6 (O)	P6 (BIO)	PIXD6 (I)	–	–	I/O
168	BIOSA7 (O)	P7 (BIO)	PIXD7 (I)	–	–	I/O
170	BIOSA8 (O)	BLANK# (BIO)	HREF (I)	–	–	I/O

Table 1-10. Pins with Multiple Uses (Ordered by Pin Number) *(cont.)*

Pin Number	BIOS ROM	Pass-through Connector	V-Port™	GPIO	Other	Pin Diagram
171	–	DCLK (BIO)	PIXCLK (I)	–	–	I/O
178	BIOSA10 (O)	–	–	GPIORD# (O)	–	O
179	BIOSA9 (O)	–	–	GPIOWR# (O)	–	O
180	BIOSA11 (O)	–	–	GPIOAS# (O)	–	O
181	–	–	–	GPIOCS# (O)	–	O
182	BIOSD0 (I)	–	–	GPIOD0 (BIO)	CONFIG1, IN0 (I)	I/O
183	BIOSD1 (I)	–	–	GPIOD1 (BIO)	CONFIG2	I/O
184	BIOSD2 (I)	–	–	GPIOD2 (BIO)	CONFIG3	I/O
185	BIOSD3 (I)	–	–	GPIOD3 (BIO)	CONFIG4	I/O
187	BIOSD4 (I)	–	–	GPIOD4 (BIO)	CONFIG5	I/O
188	BIOSD5 (I)	–	–	GPIOD5 (BIO)	CONFIG6	I/O
189	BIOSD6 (I)	–	–	GPIOD6 (BIO)	CONFIG7, OUT0 (O)	I/O
190	BIOSD7 (I)	–	–	GPIOD7 (BIO)	OUT1 (O)	I/O

2. FUNCTIONAL DESCRIPTION

2.1 General

The CL-GD5480 offers a VGA solution that is totally compatible with the IBM VGA standard. The CL-GD5480 includes a VGA core, 64-bit BitBLT engine, video capture and display, and on-board frequency synthesizers and palette DAC. A complete VGA motherboard solution can be implemented by using a single SGRAM with the CL-GD5480. Figure 2-1 is a functional block diagram of the CL-GD5480.

2.2 Functional Blocks

The following sections describe functional blocks that are integrated into the CL-GD5480.

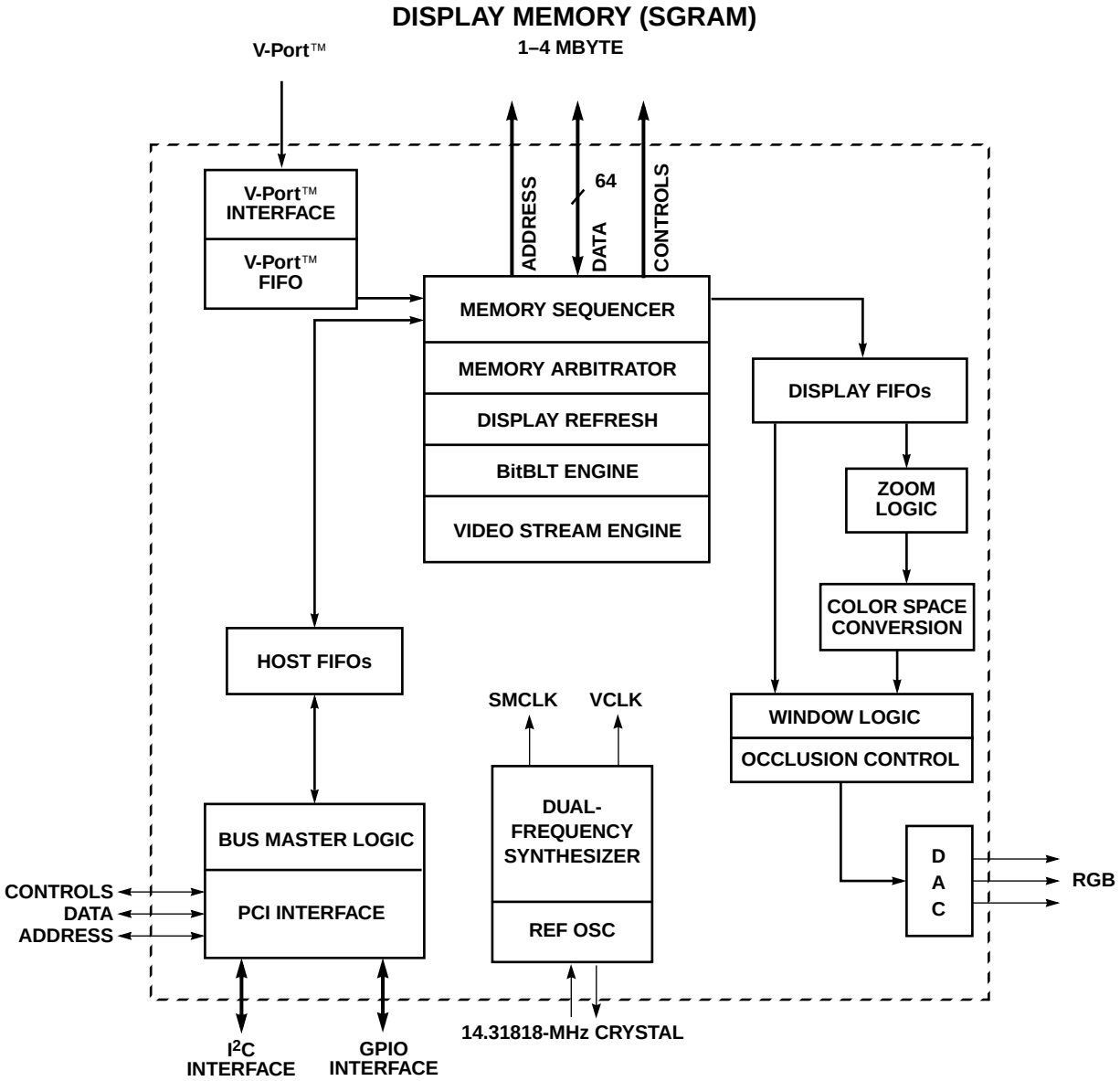


Figure 2-1. CL-GD5480 Functional Block Diagram

2.2.1 PCI Interface

The CL-GD5480 connects directly to the PCI bus with no glue logic. The CL-GD5480 decodes the entire 32-bit address so that no address mirroring or aliasing occurs. The CL-GD5480 supports single-cycle memory burst operations. The CL-GD5480 can support an additional peripheral device while remaining fully compliant with the PCI single-load specification. The CL-GD5480 is PCI 2.1-compliant.

2.2.2 Bus Master Logic

The CL-GD5480 incorporates bus master logic, using a page table in the frame buffer for memory management.

Currently, the bus master logic is used for the video stream engine, allowing data to be transferred from the frame buffer to system memory without host intervention. The bus master logic can also be used for Direct3D Z-buffer initialization.

2.2.3 CPU FIFOs

The CL-GD5480 has multi-level 64-bit CPU FIFOs that dramatically increase bandwidth across the PCI bus by allowing burst operations. The CPU write FIFO contains a queue of CPU write accesses to display memory or the BitBLT engine that have not been executed because frame buffer bandwidth has not yet been made available. Maintaining a queue allows the CL-GD5480 to generate TRDY# to complete the bus cycle as soon as it has recorded the address and data, and then to execute the operation when display memory cycles are available.

2.2.4 VGA Core

The CL-GD5480 incorporates VGA core logic to provide compatibility with older software (including compatibility testing programs).

The graphics controller is located between the CPU interface and the memory sequencer. It performs text manipulation, data rotation, color mapping, and miscellaneous operations. These operations are typically performed in the graphics controller for VGA-compatible applications; newer applications take advantage of the BitBLT engine.

The CRT controller generates all the timing required by the monitor including HSYNC, VSYNC, and BLANK#. The sync signals have programmable polarity and can be forced static for monitor power management. The CL-GD5480 BIOS supports all standard VGA modes, as well as extended resolutions up to 1600 × 1200. The CL-GD5480 supports hardware video windows for video playback.

The attribute controller formats the display for the screen (primarily text modes). Display color selection, text blinking, and underlining are performed by the attribute controller. Alternate font selection also occurs in the attribute controller.

2.2.5 Memory Arbitrator

The memory arbitrator allocates bandwidth to the various functions that compete for the frame buffer bandwidth: SGRAM refresh, screen refresh, V-Port writes, and CPU, BitBLT, and stream engine access.

SGRAM refresh is handled invisibly by performing a selectable number of refresh cycles at the beginning of each scanline. Screen refresh, V-Port writes, and CPU/BitBLT access are allocated cycles according to the FIFO control parameters. Priority is given to screen refresh and V-Port writes.

2.2.6 Memory Sequencer

The memory sequencer generates timing for display memory. The CL-GD5480 is configured to generate timing optimized for SGRAMS. The memory clock is programmable up to 100 MHz. The control signals from the CL-GD5480 to the SGRAM are RAS#, CAS#, WE#, DQM[7:0], CS#, and the multiplexed address bus. The memory data interface is either 32 or 64 bits wide.

2.2.7 BitBLT Engine

The CL-GD5480 has a 64-bit BitBLT engine that supports color expansion with or without transparency for all graphics pixel sizes as well as transparency without color expansion for 8- and 16-bpp graphics formats (source transparency).

The control registers for the BitBLT engine are memory-mapped and double-buffered. Memory-mapping the Control registers allows the fastest

possible parameter transfer. Double-buffered control registers and the autostart feature provide the greatest possible degree of parallelism between the host and the BitBLT engine.

The BitBLT engine on the CL-GD5480 supports X-Y addressing to relieve the application or the driver of time-consuming calculations of addresses in the frame buffer. In addition, it also supports an X-Y clipping rectangle. Autonomous execution of a command list maximizes CPU-VGA parallel operation.

The BitBLT engine has a dedicated set of memory apertures. This allows a system-to-screen BitBLT to proceed concurrently with a process requiring frame buffer accesses with no interference.

Each of these features of the BitBLT engine are covered in detail in Chapter 9 of the Technical Reference Manual.

2.2.8 Display FIFOs

The display FIFOs allow data from the frame buffer to be fetched before it is actually needed for screen refresh. This allows the fetches to be executed as synchronous burst read cycles rather than random read cycles, greatly increasing the available memory bandwidth. The CL-GD5480 has multiple display FIFOs, allowing information from two independent sources streams to be mixed together in the display pipeline on a pixel-by-pixel basis.

2.2.9 Window Logic and Occlusion Support

The CL-GD5480 features two programmable hardware windows for the simultaneous display of graphics and two video streams. The graphics and video formats can have different color spaces and even pixel sizes. The display of 8-bpp palettized graphics with YUV 4:2:2 video is a typical application.

The primary window can be zoomed in the horizontal and vertical directions up to 4×. Horizontal zooming is always done with interpolation of 'in-between' pixels. Vertical zooming can be done with scanline replication or scanline interpolation. In addition to zooming, the primary window can also be programmed for shrink.

Occlusion support allows the graphics and video streams to be mixed on a pixel-by-pixel basis. Color key matching of the graphics source or chroma key matching of the video source can be used to determine which pixels are replaced. Occlusion and Y-interpolation is supported for 8-, 16-, and 24-bpp graphics.

2.2.10 V-Port™

The CL-GD5480 V-Port writes real-time or recorded video from a decoder to the frame buffer, typically for display in the video window. Video can be decimated vertically, horizontally, and temporally. When video is being captured for display in the window, the capture and display buffers can be automatically swapped as each frame is captured. This prevents the display or capture of partial frames with no host intervention.

The CL-GD5480 has an independent capture FIFO. This allows video capture to occur at the same time interpolated Y-zooming and occlusion is being used for the display window.

Luminance-only capture is available for TeleText and closed caption with suitable software. Independent control of VBI region allows for seamless Intercast capture.

The V-Port hardware interface uses the same pins as the VGA pass-through connector. It can be configured for either active sense of HREF.

2.2.11 Video Stream Engine

The CL-GD5480 incorporates a video stream engine that uses the bus master logic to transfer data from the frame buffer to the system memory with a minimum of host intervention. The stream engine uses two sets of buffer pointers and can be easily synchronized with the video capture logic.

2.2.12 Palette DAC

The palette DAC block contains the color palette and three 8-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts an 8-bit color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

Alternatively, the CL-GD5480 can be configured for 15-, 16-, or 24-bit direct color RGB pixels. This

allows 32K, 64K, or 16M simultaneous colors to be displayed on the screen. The palette has independent read access for the three colors and can be used for gamma correction in direct color modes.

The CL-GD5480 also supports YUV 4:2:2, YUV 4:2:0, and AccuPak formats within the video window.

The palette DAC supports a Power-Down mode, which temporarily turns off clocks to the palette and power to the DAC to conserve power.

2.2.13 Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the memory sequencer and display clocks from a single reference frequency. The frequency of each clock is independently programmable. The maximum memory sequencer clock and display clock are 100 MHz and 135 MHz, respectively. Clock doubling allows pixel frequencies of up to 200 MHz. The reference frequency of 14.31818 MHz can be generated on-chip using an inexpensive 2-pin crystal or it can be supplied from an external TTL source.

2.2.14 VESA®/VGA Pass-Through Connector

The CL-GD5480 can connect directly to a VESA connector for output only. The device supports the three enable/disable inputs; the Pixel bus can drive the connector directly.

2.2.15 General-Purpose I/O Port

The CL-GD5480 can support an additional peripheral device on its adapter card. Address decoding and data buffering allow the additional device while maintaining the PCI 'single-load' specification.

2.2.16 I²C Interface

The CL-GD5480 has a built-in, 2-pin interface that can be used to control peripheral devices such as TV tuners, TV decoders, digital cameras, and hardware Teletext decoders. This interface can also be used for DDC2B monitor identification.

2.3 Performance

The CL-GD5480 is designed with the following performance-enhancing features:

- 64-bit SGRAM display memory data bus for faster access to display memory
- Memory-mapped, double-buffered BitBLT registers with autostart maximizes host/BitBLT overlap
- Transparent source BitBLT for increased BitBLT functionality
- 100-MHz MCLK provides 800-Mbyte/sec. peak frame-buffer bandwidth
- Burst host bus performance and a CPU write buffer that allows faster CPU access for writes to display memory
- Increased throughput with PCI local bus interface with Burst mode
- 32-bit CPU interface to display memory for faster host access in all modes, including Planar mode
- 16- or 32-bit CPU interface to I/O registers for faster host access
- Multi-level, 32-bit system memory write cache
- 32-bit internal data inputs for internal DAC
- Multiple display FIFOs to minimize memory contention
- Video capture filtered decimation to reduce the memory bandwidth requirements
- YUV 4:2:0 reduce CODEC CPU processing, increasing host bus and memory bus transfer rates
- 32 × 32 and 64 × 64 hardware cursor to improve Microsoft® Windows® performance

2.4 Board Testability

The CL-GD5480 device is testable, even when installed on a printed circuit board. By using Pin-Scan testing, any IC signal pin not connected to the board or shorted to a neighboring pin or trace, is detected (see Appendix B7, "Pin Scan", in the *CL-GD5480 Technical Reference Manual*). The signature generator allows the entire system, including the display memory, to be tested at speed (see Appendix B6, "Signature Generator", in the *CL-GD5480 Technical Reference Manual*). The CL-GD5480 enhanced signature generator test allows the BitBLT engine, the V-Port, as well as the frame buffer to be tested.

3. CONFIGURATION TABLES

3.1 Display Modes

Table 3-1. IBM® Standard VGA Display Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0, 1	0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
6	6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	7	Monochrome	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
E	E	16/256K	80 × 25	8 × 14	640 × 200	Graphics	25	31.5	70
F	F	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12	12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
13	13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70

NOTE: The EGA-compatible text modes (using an 8 × 14 font) and graphics modes 10 and F use a 16-dot high font, with the bottom two lines truncated, in the absence of TSRFONT (8 × 14 font TSR). This creates some errors when displaying characters with descenders, but does not restrict operation of programs using these modes. In text modes using the 8 × 14 font, the characters ‘g’, ‘j’, ‘p’, ‘q’, ‘y’, and ‘ÿ’ are truncated using a middle- and bottom-line algorithm to avoid truncation of descenders. For compatibility with some DOS applications using the 8 × 14 font, the TSRFONT utility should be used. Applications, such as DOSSHELL in Graphics 25 or 34 line display modes, require the TSRFONT utility to be loaded.

Table 3-2. Cirrus Logic Extended Display Modes

Mode No.	VESA® No.	Screen Resolution	No. of Colors	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz	MIN FB[4]	Note
5E	100	640 × 400	256P	25	31.5	70	1M	–
5F	101	640 × 480	256P	25	31.5	60	1M	–
5F	101	640 × 480	256P	31.5	37.9	72	1M	–
5F	101	640 × 480	256P	31.5	37.5	75	1M	–
5F	101	640 × 480	256P	36	43.3	85	1M	–
5F	101	640 × 480	256P	43.2	50.9	100	1M	GTF
66	110	640 × 480	32K	25	31.5	60	1M	–
66	110	640 × 480	32K	31.5	37.9	72	1M	–
66	110	640 × 480	32K	31.5	37.5	75	1M	–
66	110	640 × 480	32K	36	43.3	85	1M	–
66	110	640 × 480	32K	43.2	50.9	100	1M	GTF
64	111	640 × 480	64K	25	31.5	60	1M	–
64	111	640 × 480	64K	31.5	37.9	72	1M	–
64	111	640 × 480	64K	31.5	37.5	75	1M	–
64	111	640 × 480	64K	36	43.3	85	1M	–
64	111	640 × 480	64K	43.2	50.9	100	1M	GTF
71	112	640 × 480	16M	25	31.5	60	1M	–
71	112	640 × 480	16M	31.5	37.9	72	1M	–
71	112	640 × 480	16M	31.5	37.5	75	1M	–
71	112	640 × 480	16M	36	43.3	85	1M	–
71	112	640 × 480	16M	43.2	50.9	100	1M	GTF
58, 6A	102	800 × 600	16P	36	35.2	56	1M	–
58, 6A	102	800 × 600	16P	40	37.8	60	1M	–
58, 6A	102	800 × 600	16P	50	48.1	72	1M	–
58, 6A	102	800 × 600	16P	49.5	46.9	75	1M	–
5C	103	800 × 600	256P	36	35.2	56	1M	–
5C	103	800 × 600	256P	40	37.9	60	1M	–
5C	103	800 × 600	256P	50	48.1	72	1M	–
5C	103	800 × 600	256P	49.5	46.9	75	1M	–
5C	103	800 × 600	256P	56.25	53.7	85	1M	–
5C	103	800 × 600	256P	68.2	63.6	100	1M	GTF

Table 3-2. Cirrus Logic Extended Display Modes *(cont.)*

Mode No.	VESA® No.	Screen Resolution	No. of Colors	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz	MIN FB[4]	Note
67	113	800 × 600	32K	36	35.2	56	1M	–
67	113	800 × 600	32K	40	37.8	60	1M	–
67	113	800 × 600	32K	50	48.1	72	1M	–
67	113	800 × 600	32K	49.5	46.9	75	1M	–
67	113	800 × 600	32K	56.25	53.7	85	1M	–
67	113	800 × 600	32K	68.2	63.6	100	1M	GTF
65	114	800 × 600	64K	36	35.2	56	1M	–
65	114	800 × 600	64K	40	37.8	60	1M	–
65	114	800 × 600	64K	50	48.1	72	1M	–
65	114	800 × 600	64K	49.5	46.9	75	1M	–
65	114	800 × 600	64K	56.25	53.7	85	1M	–
65	114	800 × 600	64K	68.2	63.6	100	1M	GTF
78	115	800 × 600	16M	36	35.2	56	2M	–
78	115	800 × 600	16M	40	37.8	60	2M	–
78	115	800 × 600	16M	50	48.1	72	2M	–
78	115	800 × 600	16M	49.5	46.9	75	2M	–
78	115	800 × 600	16M	56.25	53.7	85	2M	–
78	115	800 × 600	16M	68.2	63.6	100	2M	GTF
5D†	104	1024 × 768	16P	44.9	35.5	43i†	1M	–
5D	104	1024 × 768	16P	65	48.3	60	1M	–
5D	104	1024 × 768	16P	75	56	70	1M	–
5D	104	1024 × 768	16P	78.7	60	75	1M	–
60†	105	1024 × 768	256P	44.9	35.5	43i†	1M	–
60	105	1024 × 768	256P	65	48.3	60	1M	–
60	105	1024 × 768	256P	75	56	70	1M	–
60	105	1024 × 768	256P	78.7	60	75	1M	–
60	105	1024 × 768	256P	94.5	68.3	85	1M	–
60	105	1024 × 768	256P	113.3	81.4	100	1M	GTF
68†	116	1024 × 768	32K	44.9	35.5	43i†	2M	–
68	116	1024 × 768	32K	65	48.3	60	2M	–
68	116	1024 × 768	32K	75	56	70	2M	–

Table 3-2. Cirrus Logic Extended Display Modes *(cont.)*

Mode No.	VESA® No.	Screen Resolution	No. of Colors	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz	MIN FB[4]	Note
68	116	1024 × 768	32K	78.7	60	75	2M	–
68	116	1024 × 768	32K	94.5	68.3	85	2M	–
68	116	1024 × 768	32K	113.3	81.4	100	2M	GTF
74	117	1024 × 768	64K	44.9	35.5	43i†	2M	–
74	117	1024 × 768	64K	65	48.3	60	2M	–
74	117	1024 × 768	64K	75	56	70	2M	–
74	117	1024 × 768	64K	78.7	60	75	2M	–
74	117	1024 × 768	64K	94.5	68.3	85	2M	–
74	117	1024 × 768	64K	113.3	81.4	100	2M	GTF
79	118	1024 × 768	16M	44.9	35.5	43i†	4M	–
79	118	1024 × 768	16M	65	48.3	60	4M	–
79	118	1024 × 768	16M	75	56	70	4M	–
79	118	1024 × 768	16M	78.7	60	75	4M	–
79	118	1024 × 768	16M	94.5	68.3	85	4M	–
79	118	1024 × 768	16M	113.3	81.4	100	4M	GTF
7C	–	1152 × 864	256P	94.5	63.9	70	1M	–
7C	–	1152 × 864	256P	108	67.5	75	1M	–
7C	–	1152 × 864	256P	121.5	76.7	85	1M	–
7C	–	1152 × 864	256P	143.5	91.5	100	1M	GTF
6E	–	1152 × 864	32K	94.5	63.9	70	2M	–
6E	–	1152 × 864	32K	108	67.5	75	2M	–
6E	–	1152 × 864	32K	121.5	76.7	85	2M	–
6E	–	1152 × 864	32K	143.5	91.5	100	2M	GTF
7D	–	1152 × 864	64K	94.5	63.9	70	2M	–
7D	–	1152 × 864	64K	108	67.5	75	2M	–
7D	–	1152 × 864	64K	121.5	76.7	85	2M	–
7D	–	1152 × 864	64K	143.5	91.5	100	2M	GTF
7E	–	1152 × 864	16M	94.5	63.9	70	4M	–
7E	–	1152 × 864	16M	108	67.5	75	4M	–
7E	–	1152 × 864	16M	121.5	76.7	85	4M	–
6C†	106	1280 × 1024	16P	75	48	43i†	1M	–

Table 3-2. Cirrus Logic Extended Display Modes *(cont.)*

Mode No.	VESA® No.	Screen Resolution	No. of Colors	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz	MIN FB[4]	Note
6D†	107	1280 × 1024	256P	75	48	43i†	2M	–
6D	107	1280 × 1024	256P	108	65	60	2M	–
6D	107	1280 × 1024	256P	135	80	75	2M	–
6D	107	1280 × 1024	256P	157.5	91	85	2M	–
69†	119	1280 × 1024	32K	75	48	43i†	4M	–
69	119	1280 × 1024	32K	108	65	60	4M	–
69	119	1280 × 1024	32K	135	80	75	4M	–
69	119	1280 × 1024	32K	157.5	91	85	4M	–
75	11A	1280 × 1024	64K	75	48	43i†	4M	–
75	11A	1280 × 1024	64K	108	63.9	60	4M	–
75	11A	1280 × 1024	64K	135	80	75	4M	–
75	11A	1280 × 1024	64K	157.5	91	85	4M	–
77	11B	1280 × 1024	16M	75	48	43i	4M	–
77	11B	1280 × 1024	16M	108	63.9	60	4M	–
7B	–	1600 × 1200	256P	135	62.5	48i	2M	–
7B	–	1600 × 1200	256P	162	75	60	2M	–
6F	–	1600 × 1200	32K	135	62.5	48i	4M	–
6F	–	1600 × 1200	32K	162	75	60	4M	–
7F	–	1600 × 1200	64K	135	62.5	48i	4M	–
7F	–	1600 × 1200	64K	162	75	60	4M	–

NOTES:

1) '†' character indicates Interlaced mode.
2) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected is automatically used.
3) GTF indicates the pixel frequency and horizontal frequency were calculated with the VESA *Generalized Timing Formula* proposal, v1 Rev. 0.5.
4) 'FB' indicates frame buffer.

4. VGA REGISTER PORT MAP

Table 4-1. VGA Register Port Map

Address	Port
3B4	CRT Controller Index (R/W — monochrome)
3B5	CRT Controller Data (R/W — monochrome)
3BA	Feature Control (W), Input Status Register 1 (R — monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status Register 0 (R)
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register (R/W)
3C7	Pixel Address Read Mode (W), DAC State (R)
3C8	Pixel Mask Write Mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3D4	CRT Controller Index (R/W — color)
3D5	CRT Controller Data (R/W — color)
3DA	Feature Control (W), Input Status Register 1 (R — color)

5. REGISTER MAP

All CL-GD5480 registers are listed in Table 5-1. Page numbers in the Page column refer to the register description chapters in the *CL-GD5480 Technical Reference Manual*. Registers at I/O port 3Dxh are at 3Bxh when the CL-GD5480 is programmed for Monochrome mode (MISC[0]).

Table 5-1. CL-GD5480 Registers

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
ARX	Attribute Controller Index	3C0/3C1h	–	00h/01h	4-69
AR0–ARF	Attribute Controller Palette	3C0/3C1h	0h–0Fh	00h/01h	4-70
AR10	Attribute Controller Mode	3C0/3C1h	10h	00h/01h	4-71
AR11	Overscan (Border) Color	3C0/3C1h	11h	00h/01h	4-73
AR12	Color Plane Enable	3C0/3C1h	12h	00h/01h	4-74
AR13	Pixel Panning	3C0/3C1h	13h	00h/01h	4-75
AR14	Color Select	3C0/3C1h	14h	00h/01h	4-76
CRX	CRTC Index	3D4h	–	14h	4-23
CR0	CRTC Horizontal Total	3D5h	00h	15h	4-26
CR1	CRTC Horizontal Display End	3D5h	01h	15h	4-27
CR2	CRTC Horizontal Blanking Start	3D5h	02h	15h	4-28
CR3	CRTC Horizontal Blanking End	3D5h	03h	15h	4-29
CR4	CRTC Horizontal Sync Start	3D5h	04h	15h	4-31
CR5	CRTC Horizontal Sync End	3D5h	05h	15h	4-32
CR6	CRTC Vertical Total	3D5h	06h	15h	4-34
CR7	CRTC Overflow	3D5h	07h	15h	4-35
CR8	CRTC Screen A Preset Row-Scan	3D5h	08h	15h	4-36
CR9	CRTC Character Cell Height	3D5h	09h	15h	4-37
CRA	CRTC Text Cursor Start	3D5h	0Ah	15h	4-38
CRB	CRTC Text Cursor End	3D5h	0Bh	15h	4-39
CRC	CRTC Screen Start Address High	3D5h	0Ch	15h	4-40
CRD	CRTC Screen Start Address Low	3D5h	0Dh	15h	4-41
CRE	CRTC Text Cursor Location High	3D5h	0Eh	15h	4-42
CRF	CRTC Text Cursor Location Low	3D5h	0Fh	15h	4-43
CR10	CRTC Vertical Sync Start	3D5h	10h	15h	4-44
CR11	CRTC Vertical Sync End	3D5h	11h	15h	4-45
CR12	CRTC Vertical Display End	3D5h	12h	15h	4-47

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
CR13	CRTC Offset (Pitch)	3D5h	13h	15h	4-48
CR14	CRTC Underline Row Scanline	3D5h	14h	15h	4-49
CR15	CRTC Vertical Blank Start	3D5h	15h	15h	4-50
CR16	CRTC Vertical Blank End	3D5h	16h	15h	4-51
CR17	CRTC Mode Control	3D5h	17h	15h	4-52
CR18	CRTC Line Compare	3D5h	18h	15h	4-54
CR19	Interlace End	3D5h	19h	15h	8-41
CR1A	Miscellaneous Control	3D5h	1Ah	15h	8-42
CR1B	Extended Display Controls	3D5h	1Bh	15h	8-43
CR1C	Sync Adjust and Genlock	3D5h	1Ch	15h	8-45
CR1D	Overlay Extended Control	3D5h	1Dh	15h	8-47
CR1E	Bus Master Page Table Start Address Byte 1	3D5h	1Eh	15h	8-48
CR1F	Bus Master Page Table Start Address Byte 2	3D5h	1Dh	15h	8-48
CR22	Graphics Data Latches Readback	3D5h	22h	15h	4-55
CR24	Attribute Controller Toggle Readback (read only)	3D5h	24h	15h	4-56
CR25	Part Status (read only)	3D5h	25h	15h	8-49
CR26	Attribute Controller Index Readback	3D5h	26h	15h	4-57
CR27	ID (read only)	3D5h	27h	15h	8-50
CR31	Window 1 Horizontal Zoom Control	3D5h	31h	15h	6-5
CR32	Window 1 Vertical Zoom Control	3D5h	32h	15h	6-6
CR33	Window 1 Horizontal Region 1 Size	3D5h	33h	15h	6-7
CR34	Window 1 Region 2 Width	3D5h	34h	15h	6-8
CR35	Window 1 Region 2 Source Data Size	3D5h	35h	15h	6-9
CR36	Window 1 Horizontal Overflow	3D5h	36h	15h	6-10
CR37	Window 1 Vertical Start	3D5h	37h	15h	6-11
CR38	Window 1 Vertical End	3D5h	38h	15h	6-12
CR39	Window 1 Vertical Overflow	3D5h	39h	15h	6-13
CR3A	Window 1 Source Address Byte 0	3D5h	3Ah	15h	6-15
CR3B	Window 1 Source Address Byte 1	3D5h	3Bh	15h	6-15
CR3C	Window 1 Source Address Byte 2	3D5h	3Ch	15h	6-16
CR3D	Video Buffer Address Offset	3D5h	3Dh	15h	6-17

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
CR3E	Window 1 Master Control	3D5h	3Eh	15h	6-18
CR3F	Miscellaneous Video Control	3D5h	3Fh	15h	6-20
CR40	Window 2 Pixel Alignment	3D5h	40h	15h	6-22
CR43	Window 2 Horizontal Region 1 Size	3D5h	43h	15h	6-23
CR44	Window 2 Region 2 Width	3D5h	44h	15h	6-24
CR45	Window 2 Region 2 Source Data Size	3D5h	45h	15h	6-25
CR46	Window 2 Horizontal Overflow	3D5h	46h	15h	6-26
CR47	Window 2 Vertical Start	3D5h	47h	15h	6-27
CR48	Window 2 Vertical End	3D5h	48h	15h	6-28
CR49	Window 2 Vertical Overflow	3D5h	49h	15h	6-29
CR4A	Window 2 Start Address Byte 0	3D5h	4Ah	15h	6-30
CR4B	Window 2 Start Address Byte 1	3D5h	4Bh	15h	6-30
CR4C	Window 2 Start Address Byte 2	3D5h	4Ch	15h	6-31
CR4D	Window 2 Buffer Address Offset	3D5h	4Dh	15h	6-32
CR4E	Window 2 Control	3D5h	4Eh	15h	6-33
CR4F	Window 2 Miscellaneous Control	3D5h	4Fh	15h	6-34
CR50	Video Capture Control	3D5h	50h	15h	6-35
CR51	Video Capture Data Format	3D5h	51h	15h	6-37
CR52	Video Capture Buffers 1 and 2 Horizontal Shrink	3D5h	52h	15h	6-38
CR53	Video Capture Buffers 1 and 2 Vertical Shrink	3D5h	53h	15h	6-39
CR54	Video Capture Horizontal Delay	3D5h	54h	15h	6-40
CR55	Video Capture Horizontal Width	3D5h	55h	15h	6-41
CR56	Video Capture Vertical Delay	3D5h	56h	15h	6-42
CR57	Video Capture Maximum Height	3D5h	57h	15h	6-43
CR58	Video Capture Miscellaneous Control	3D5h	58h	15h	6-44
CR59	Video Capture Buffer 1 Start Address Byte 0	3D5h	59h	15h	6-45
CR5A	Video Capture Buffer 1 Start Address Byte 1	3D5h	5Ah	15h	6-45
CR5B	Video Window Brightness Adjust	3D5h	5Bh	15h	6-46
CR5C	Luminance-Only Capture Control	3D5h	5Ch	15h	6-47
CR5D	Window 1 Pixel Alignment	3D5h	5Dh	15h	6-48
CR5E	Double-Buffer Control	3D5h	5Eh	15h	6-49

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
CR5F	Video Capture Clipping Overflow	3D5h	5Fh	15h	6-51
CR60	Window 1 Source 2 Start Address Byte 0	3D5h	60h	15h	6-52
CR61	Window 1 Source 2 Start Address Byte 1	3D5h	61h	15h	6-52
CR62	Interrupt Source and Status	3D5h	62h	15h	6-53
CR63	Miscellaneous Video Memory Aperture Controls	3D5h	63h	15h	6-55
CR64	Video Capture Buffer 2 Address Byte 0	3D5h	64h	15h	6-56
CR65	Video Capture Buffer 2 Address Byte 1	3D5h	65h	15h	6-56
CR66	Video Capture Buffer 2 Address Byte 2	3D5h	66h	15h	6-57
CR67	Video Capture Buffers 1 and 2 Address Offset Option	3D5h	67h	15h	6-58
CR68	Video Capture Buffer 3 Address Byte 0	3D5h	68h	15h	6-59
CR69	Video Capture Buffer 3 Address Byte 1	3D5h	69h	15h	6-59
CR6A	Video Capture Buffer 3 Address Byte 2	3D5h	6Ah	15h	6-60
CR6B	Video Capture Buffer 3 Address Offset	3D5h	6Bh	15h	6-61
CR6C	Video Capture Buffer 3 Horizontal Shrink	3D5h	6Ch	15h	6-62
CR6D	Video Capture Buffer 3 Vertical Shrink	3D5h	6Dh	15h	6-63
CR6E	Capture Line Readback	3D5h	6Eh	15h	6-64
CR6F	Video Capture Buffers Extended Controls	3D5h	6Fh	15h	6-65
CR70	Stream Engine Buffer 1 Page Table Offset	3D5h	70h	15h	6-67
CR71	Stream Engine Buffer 1 Target Address Byte 0	3D5h	71h	15h	6-68
CR72	Stream Engine Buffer 1 Source Address Byte 0	3D5h	72h	15h	6-69
CR73	Stream Engine Buffer 1 Source Address Byte 1	3D5h	73h	15h	6-69
CR74	Stream Engine Buffer 2 Page Table Offset	3D5h	74h	15h	6-70
CR75	Stream Engine Buffer 2 Target Address Byte 0	3D5h	75h	15h	6-71
CR76	Stream Engine Buffer 2 Source Address Byte 0	3D5h	76h	15h	6-72
CR77	Stream Engine Buffer 2 Source Address Byte 1	3D5h	77h	15h	6-72
CR78	Stream Engine Buffer 1 Extension Bits	3D5h	78h	15h	6-73
CR79	Stream Engine Buffer 2 Extension Bits	3D5h	79h	15h	6-74
CR7A	Stream Engine Source Buffer Offset	3D5h	7Ah	15h	6-75
CR7B	Stream Engine Destination Buffer Offset	3D5h	7Bh	15h	6-76
CR7C	Stream Engine Target Buffer Width	3D5h	7Ch	15h	6-77

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
CR7D	Stream Engine Target Buffer Height	3D5h	7Dh	15h	6-78
CR7E	Stream Engine Vertical Scaling	3D5h	7Eh	15h	6-79
CR7F	Stream Engine Controls	3D5h	7Fh	15h	6-80
FC	Feature Control (W)	3DAh	–	1Ah	4-7
FC	Feature Control (R)	3CAh	–	1Ah	4-7
FEAT	Input Status Register 0	3C2h	–	02h	4-8
GRX	Graphics Controller Index (read only)	3CEh	–	0Eh	4-58
GR0	Graphics Controller Set/Reset / Background Color Byte 0	3CFh	00h	100h	4-59
GR1	Graphics Controller Set/Reset Enable / Foreground Color Byte 0	3CFh	01h	104h	4-60
GR2	Graphics Controller Color Compare	3CFh	02h	0Fh	4-61
GR3	Graphics Controller Data Rotate	3CFh	03h	0Fh	4-62
GR4	Graphics Controller Read Map Select	3CFh	04h	0Fh	4-63
GR5	Graphics Controller Mode	3CFh	05h	0Fh	4-64
GR6	Graphics Controller Miscellaneous	3CFh	06h	0Fh	4-66
GR7	Graphics Controller Color Don’t Care	3CFh	07h	0Fh	4-67
GR8	Graphics Controller Bit Mask	3CFh	08h	0Fh	4-68
GR9	Offset Register 0	3CFh	09h	0Fh	8-24
GRA	Offset Register 1	3CFh	0Ah	0Fh	8-26
GRB	Graphics Controller Mode Extensions	3CFh	0Bh	0Fh	8-27
GRC	Color/Chroma Key Compare	3CFh	0Ch	0Fh	8-29
GRD	Color Key / Mask/ Chroma Key	3CFh	0Dh	0Fh	8-30
GRE	Power Management	3CFh	0Eh	0Fh	8-31
GR10	Background Color Byte 1	3CFh	10h	101h	5-4
GR11	Foreground Color Byte 1	3CFh	11h	105h	5-4
GR12	Background Color Byte 2	3CFh	12h	102h	5-4
GR13	Foreground Color Byte 2	3CFh	13h	106h	5-4
GR14	Background Color Byte 3	3CFh	14h	103h	5-4
GR15	Foreground Color Byte 3	3CFh	15h	107h	5-4
GR16	Active Display Line Readback Byte 0	3CFh	16h	0Fh	8-33

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
GR17	Active Display Line Readback Byte 1	3CFh	17h	0Fh	8-34
GR18	Memory Option	3CFh	18h	0Fh	8-36
GR19	GPIO Port Configuration	3CFh	19h	0Fh	8-38
GR1A	Scratch Pad 4	3CFh	1Ah	0Fh	8-39
GR1B	Scratch Pad 5	3CFh	1Bh	0Fh	8-39
GR1C	Chroma Key Byte 0	3CFh	1Ch	0Fh	6-82
GR1D	Chroma Key Byte 1	3CFh	1Dh	0Fh	6-82
GR1E	Chroma Key Byte 2	3CFh	1Eh	0Fh	6-82
GR1F	Chroma Key Byte 3	3CFh	1Fh	0Fh	6-82
GR20	BLT Width Byte 0	3CFh	20h	108h	5-5
GR21	BLT Width Byte 1	3CFh	21h	109h	5-5
GR22	BLT Height Byte 0	3CFh	22h	10Ah	5-6
GR23	BLT Height Byte 1	3CFh	23h	10Bh	5-6
GR24	BLT Destination Pitch Byte 0	3CFh	24h	10Ch	5-7
GR25	BLT Destination Pitch Byte 1	3CFh	25h	10Dh	5-7
GR26	BLT Source Pitch Byte 0	3CFh	26h	10Eh	5-8
GR27	BLT Source Pitch Byte 1	3CFh	27h	10Fh	5-8
GR28	BLT Destination Start Byte 0	3CFh	28h	110h	5-9
GR29	BLT Destination Start Byte 1	3CFh	29h	111h	5-9
GR2A	BLT Destination Start Byte 2	3CFh	2Ah	112h	5-9
GR2B	BLT Command List Offset	3CFh	2Bh	113h	5-10
GR2C	BLT Source Start Byte 0	3CFh	2Ch	114h	5-11
GR2D	BLT Source Start Byte 1	3CFh	2Dh	115h	5-11
GR2E	BLT Source Start Byte 2	3CFh	2Eh	116h	5-11
GR2F	BLT Destination Left-side Clipping	3CFh	2Fh	117h	5-12
GR30	BLT Mode	3CFh	30h	118h	5-13
GR31	BLT Start/Status	3CFh	31h	140h	5-16
GR32	BLT ROP (Raster Operation)	3CFh	32h	11Ah	5-18
GR33	BLT Mode Extensions	3CFh	33h	11Bh	5-20
GR34	Transparent BLT Key Color Byte 0	3CFh	34h	11Ch	5-22
GR35	Transparent BLT Key Color Byte 1	3CFh	35h	11Dh	5-22

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
GR38	Stream Engine Fill Value Byte 0	3CFh	38h	120h	6-83
GR39	Stream Engine Fill Value Byte 1	3CFh	39h	121h	6-83
GR3A	Stream Engine Fill Value Byte 2	3CFh	3Ah	122h	6-83
GR3B	Stream Engine Fill Value Byte 3	3CFh	3Bh	123h	6-83
GR40	BLT Destination X-Position Byte 0	3CFh	40h	128h	5-23
GR41	BLT Destination X-Position Byte 1	3CFh	41h	129h	5-23
GR42	BLT Destination Y-Position Byte 0	3CFh	42h	12Ah	5-24
GR43	BLT Destination Y-Position Byte 1	3CFh	43h	12Bh	5-24
GR44	BLT Source X-Position Byte 0	3CFh	44h	12Ch	5-25
GR45	BLT Source X-Position Byte 1	3CFh	45h	12Dh	5-25
GR46	BLT Source Y-Position Byte 0	3CFh	46h	12Eh	5-26
GR47	BLT Source Y-Position Byte 1	3CFh	47h	12Fh	5-26
GR48	BLT Clip Rectangle X-Start Byte 0	3CFh	48h	130h	5-27
GR49	BLT Clip Rectangle X-Start Byte 1	3CFh	49h	131h	5-27
GR4A	BLT Clip Rectangle Y-Start Byte 0	3CFh	4Ah	132h	5-28
GR4B	BLT Clip Rectangle Y-Start Byte 1	3CFh	4Bh	133h	5-28
GR4C	BLT Clip Rectangle X-End Byte 0	3CFh	4Ch	134h	5-29
GR4D	BLT Clip Rectangle X-End Byte 1	3CFh	4Dh	135h	5-29
GR4E	BLT Clip Rectangle Y-End Byte 0	3CFh	4Eh	136h	5-30
GR4F	BLT Clip Rectangle Y-End Byte 1	3C4h	4Fh	137h	5-30
GD7D	Hidden Graphics Extension 7D	3CDh	7Dh	–	8-40
GR7E	Hidden Graphics Extension 7E	3CEh	7Eh	–	8-40
GR7F	Hidden Graphics Extension 7F	3CFh	7Fh	–	8-40
HDR	Hidden DAC Register	3C6h	–	06h	8-51
MISC	Miscellaneous Output (W)	3C2h	–	02h	4-5
MISC	Miscellaneous Output (R)	3CCh	–	0Ch	4-5
PCI00	PCI Device/Vendor ID	00h	–	–	7-3
PCI04	PCI Status/Command	04h	–	–	7-4
PCI08	PCI Class Code	08h	–	–	7-6
PCI0C	PCI Latency Timer	0Ch	–	–	7-7
PCI10	PCI Display Memory Base Address	10h	–	–	7-8

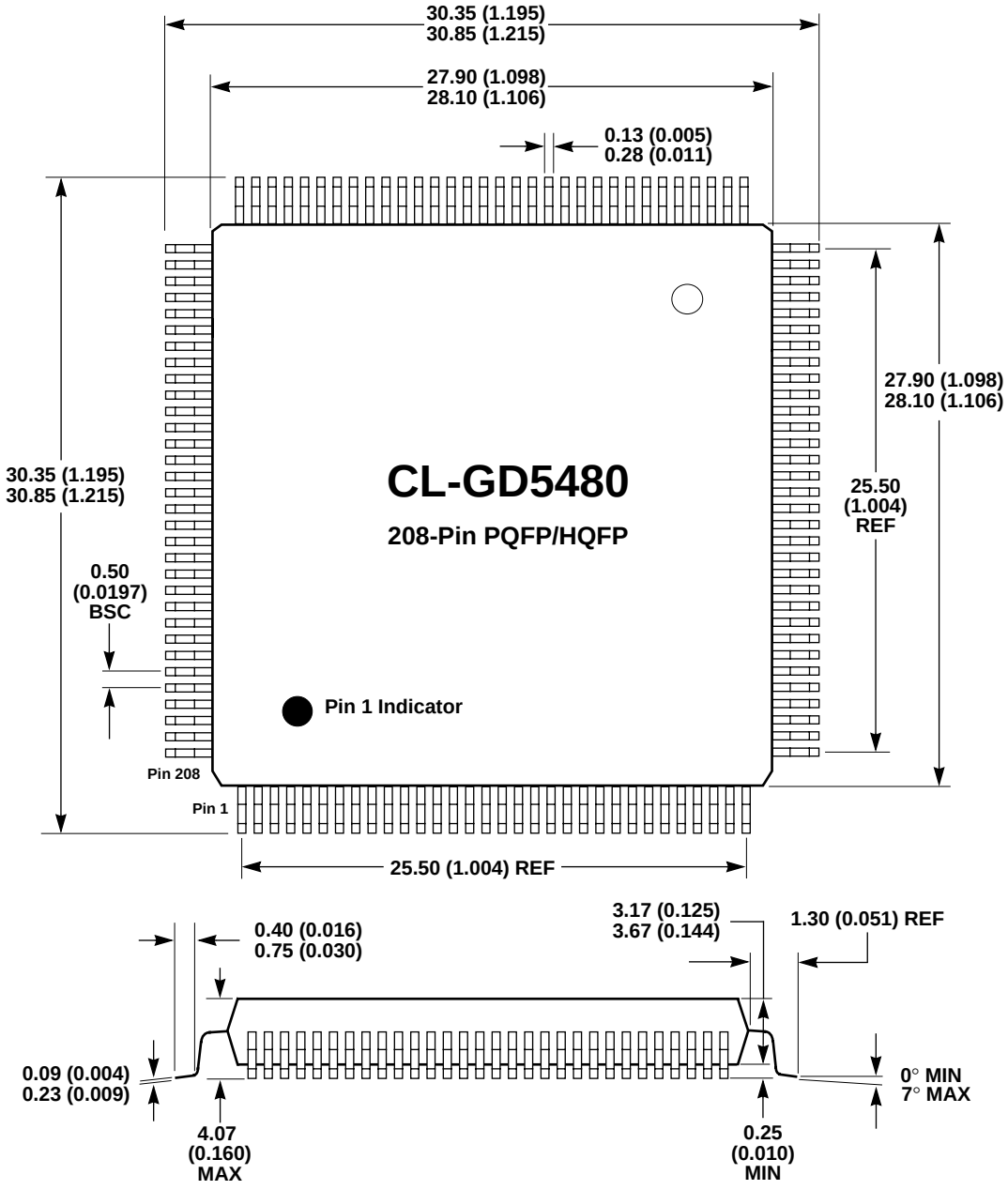
Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
PCI14	PCI VGA I/O and BitBLT Control Base Address	14h	–	–	7-9
PCI18	PCI GPIO Base Address	18h	–	–	7-10
PCI2C	PCI Subsystem/Vendor ID	2Ch	–	–	7-11
PCI30	PCI Expansion ROM Base Address	30h	–	–	7-13
PCI3C	PCI Interrupt	3Ch	–	–	7-14
SRX	Sequencer Index	3C4h	–	04h	4-15
SR0	Sequencer Reset	3C5h	00h	05h	4-16
SR1	Sequencer Clocking Mode	3C5h	01h	05h	4-17
SR2	Sequencer Plane Mask	3C5h	02h	05h	4-19
SR3	Sequencer Character Map Select	3C5h	03h	05h	4-20
SR4	Sequencer Memory Mode	3C5h	04h	05h	4-22
SR6	Key	3C5h	06h	05h	8-4
SR7	Extended Sequencer Mode	3C5h	07h	05h	8-5
SR8	I^2C Controls	3C5h	08h	05h	8-7
SR9	Scratch Pad 0	3C5h	09h	05h	8-8
SRA	Scratch Pad 1	3C5h	0Ah	05h	8-8
SRB	VCLK0 Numerator	3C5h	0Bh	05h	8-9
SRC	VCLK1 Numerator	3C5h	0Ch	05h	8-9
SRD	VCLK2 Numerator	3C5h	0Dh	05h	8-9
SRE	VCLK3 Numerator	3C5h	0Eh	05h	8-9
SRF	SGRAM Control	3C5h	0Fh	05h	8-10
SR10	Graphics Cursor X Position	3C5h	10h	05h	8-11
SR11	Graphics Cursor Y Position	3C5h	11h	05h	8-12
SR12	Graphics Cursor Attribute	3C5h	12h	05h	8-13
SR13	Graphics Cursor Pattern Address Offset	3C5h	13h	05h	8-15
SR14	Scratch Pad 2	3C5h	14h	05h	8-16
SR15	Scratch Pad 3	3C5h	15h	05h	8-16
SR16	Display FIFO Threshold Control	3C5h	16h	05h	8-17
SR17	Miscellaneous System Interface Control	3C5h	17h	05h	8-18
SR18	Signature Generator Control	3C5h	18h	05h	8-19
SR19	Signature Generator Result Low-Byte	3C5h	19h	05h	8-20

Table 5-1. CL-GD5480 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
SR1A	Signature Generator Result High-Byte	3C5h	1Ah	05h	8-21
SR1B	VCLK0 Denominator and Post-Scalar	3C5h	1Bh	05h	8-22
SR1C	VCLK1 Denominator and Post-Scalar	3C5h	1Ch	05h	8-22
SR1D	VCLK2 Denominator and Post-Scalar	3C5h	1Dh	05h	8-22
SR1E	VCLK3 Denominator and Post-Scalar	3C5h	1Eh	05h	8-22
SR1F	SMCLK Select	3C5h	1Fh	05h	8-23
STAT	Input Status Register 1	3DAh	–	1Ah	4-9
–	Pixel Mask	3C6h	–	06h	4-10
–	Palette Address (Read mode) (write only)	3C7h	–	07h	4-11
–	DAC State (read only)	3C7h	–	07h	4-12
–	Palette Address (Write mode)	3C8h	–	08h	4-13
–	Palette Data	3C9h	–	09h	4-14

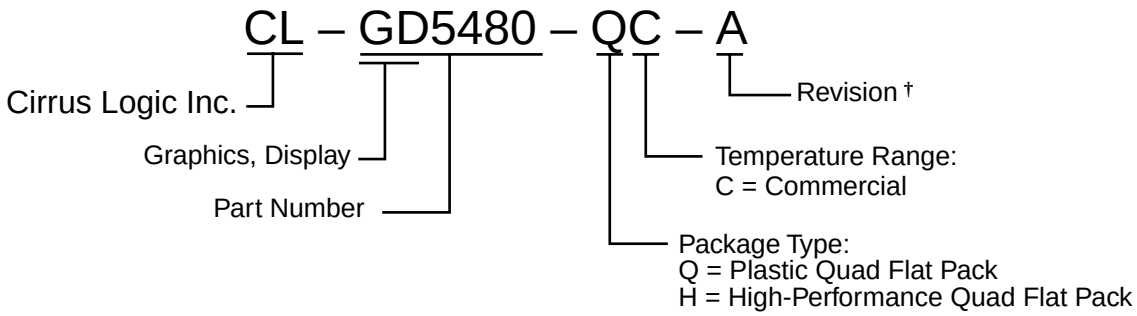
6. PACKAGE SPECIFICATIONS



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) HQFP is a high-performance QFP with an exposed or unexposed heat sink.

7. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic. for up-to-date information on revisions.

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