82C101
Single-Chip PC/XT Systems Controller

The 82C101 is a high performance CMOS PC/XT bus and peripheral controller for designers to build a PC BUS-compatible single-board computer with "turbo" power. The 82C101 replaces all TTL/SSI/MSI devices including six Intel peripheral controller ICs required to build a typical "Turbo XT." The 82C101 integrates all the controller functions of a typical "Turbo/XT" high performance motherboard. This high integration not only increases system performance but also reduces the total system cost because of lower power requirements, increased reliability, and reduced components and board size.

Features

- 100% hardware and software compatible with IBM* PC/XT
- Fully compatible with Intel's
  - 8284 Clock Generator
  - 8288 Bus Controller
  - 8237 DMA Controller
  - 8259 Interrupt Controller
  - 8254 Timer/Counter
- 8255 compatible peripheral I/O port
- Built-in parity generator and checker, wait state logic, and NMI control logic
- Supports EMS
- Supports Shadow RAM
- Supports low operating frequency for power-saving feature
- Supports 8 MHz and 10 MHz turbo speed
- Keyboard Interface
- Supports 8086 interface
- DRAM Controller for 120 ns/150 ns DRAM
- Supports five 256K x 4 DRAM to achieve 640K on board without parity
- Supports 256K x 1, 256K x 4, 1M x 1 DRAM
- Supports mixed memory
- 1.5 micron high performance CMOS technology
- TTL compatible
- 128 PQFP package

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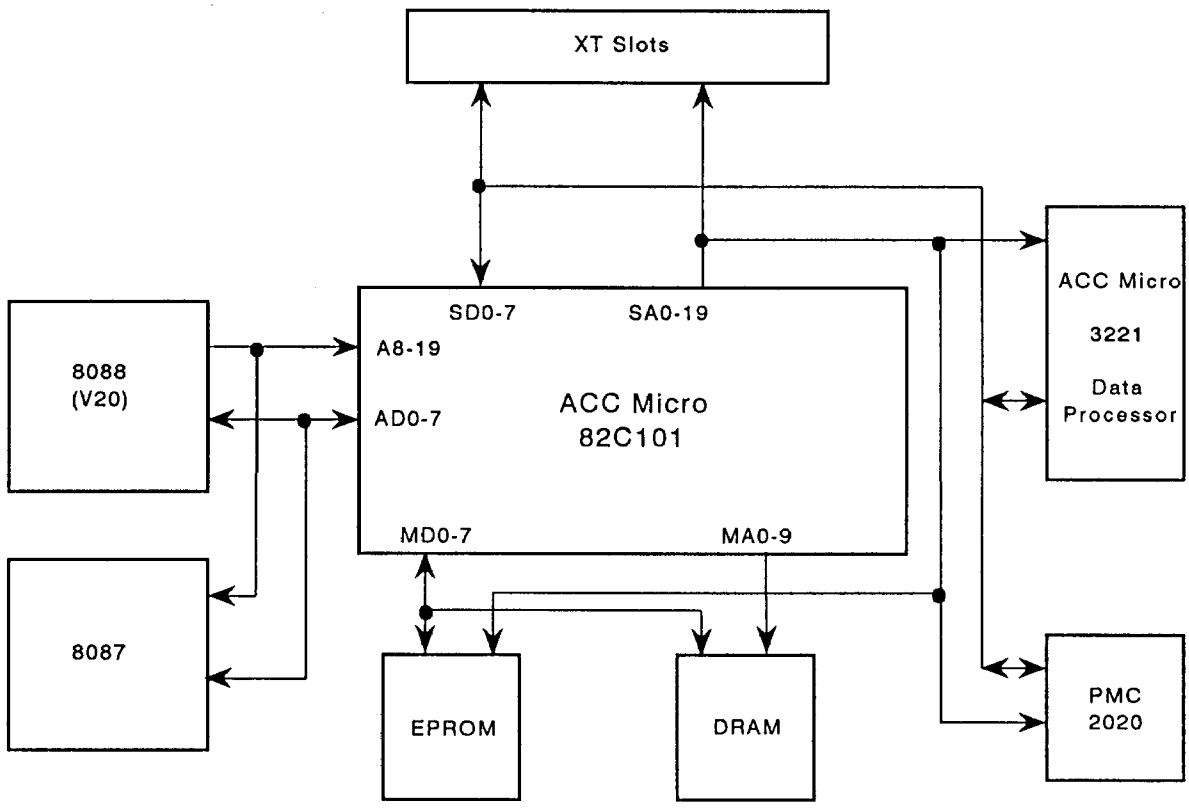
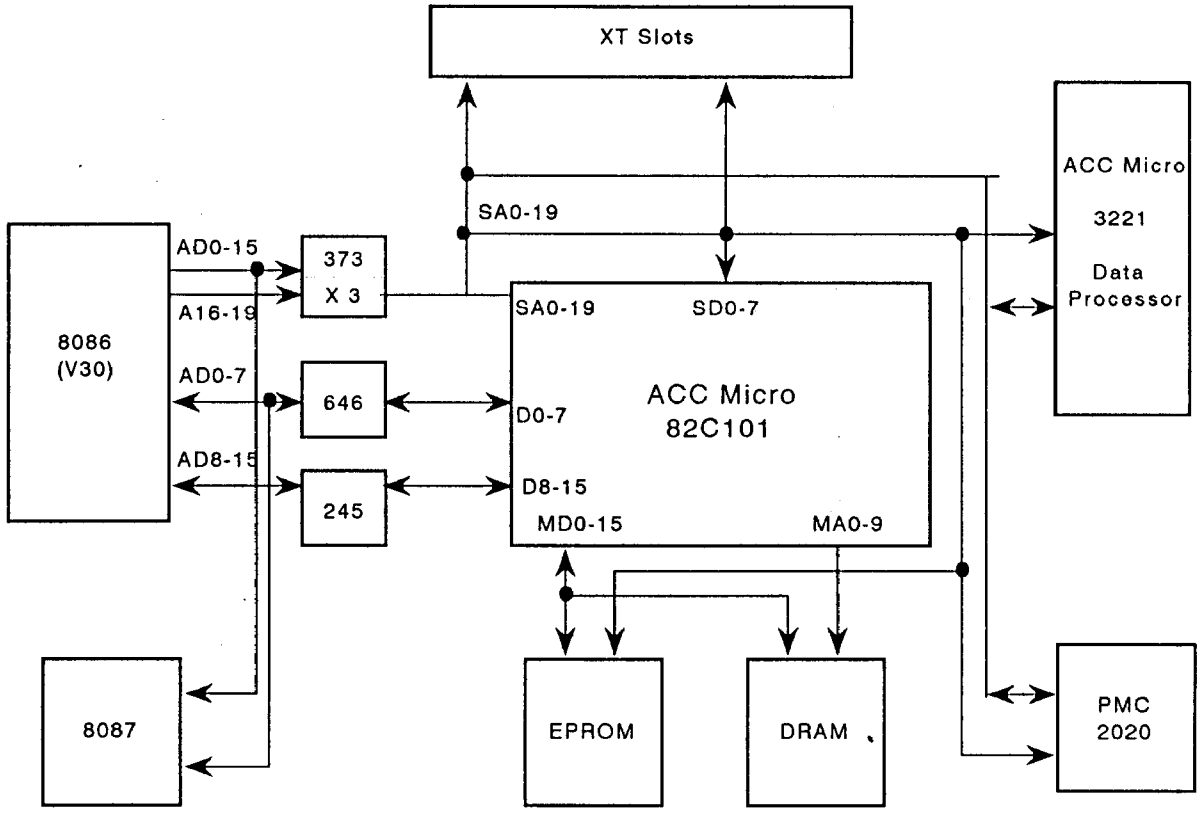
82C101 System Block Diagram

8088 Application:

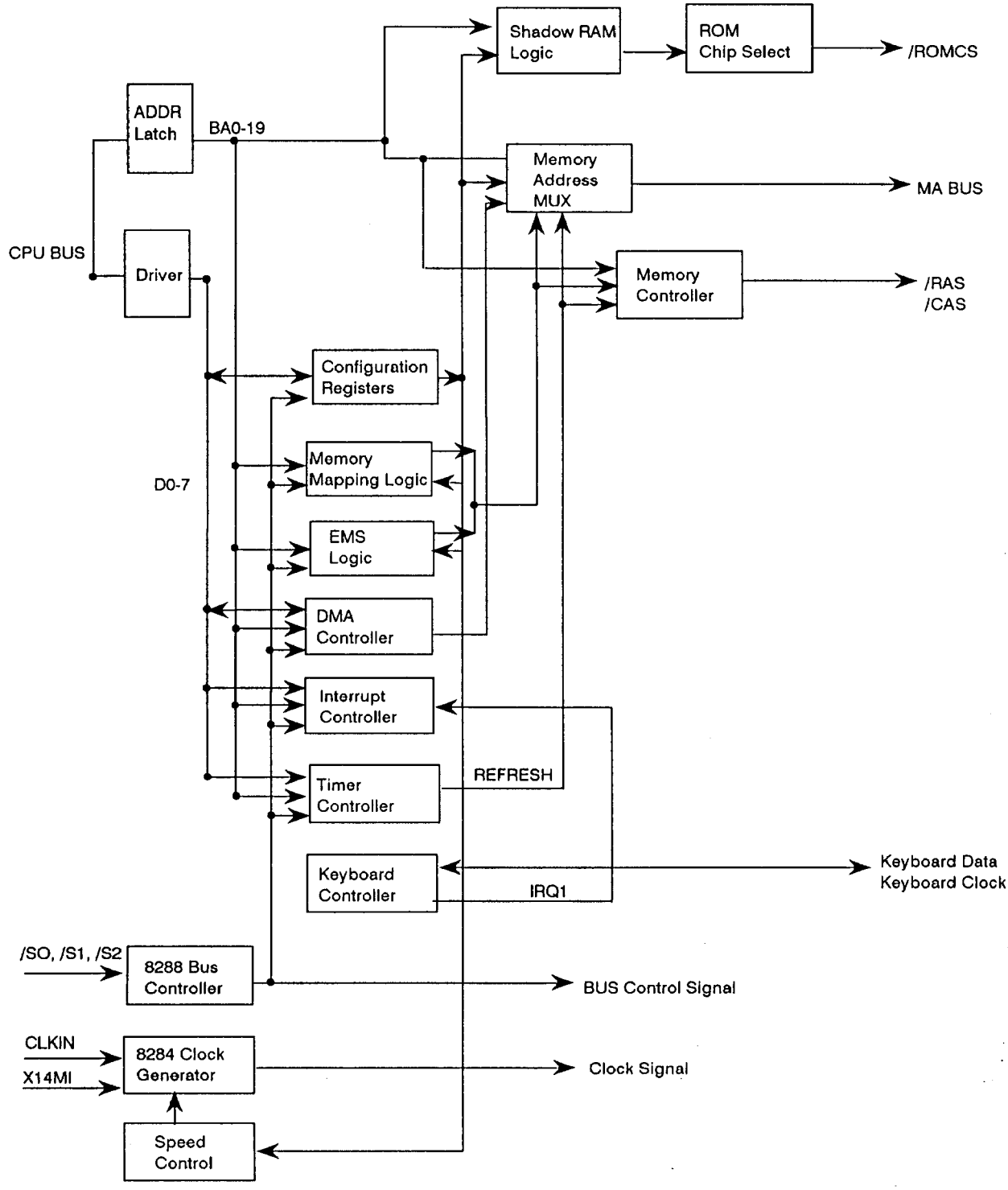


82C101 System Block Diagram

8086 Application:



ACC Micro 82C101 Functional Block Diagram



Functional Description

Clock Generator

The clock generator is functionally equivalent to Intel's 8284 clock generator. It provides clocks, ready synchronization, and reset signals to the system. With the addition of logic, two different operational frequencies are supported. One is generated from the 14.318 MHz crystal input, X14MHz. The other is from the optional oscillator input, CLKIN. The CPU clock is switched between these two inputs by CPU speed control logic. For normal speed, the CPU clock is connected to 4.77 MHz driven by X14MHz. For turbo speed, the CPU clock is one third of the frequency of CLKIN. Additional logic is also included to support two different duty cycle clocks; 33% duty cycle for Intel 808X CPUs and 50% duty cycle for NEC V20/V30 CPUs.

CPU Speed Control Logic

The CPU clock is switched between turbo and normal speed by programming bit 4 of System Configuration Register (index 2). When bit 2 of the same System Configuration Register is set to 1, CPU clock frequency is fixed at 2.385 MHz to provide power conservation, regardless what the value of bit 4 is.

Bus Controller

The 82C101 bus controller is functionally equivalent to Intel's 8288 bus controller. It provides the command generation and control signals for the internal bus and XT compatible I/O channel. When the CPU clock is at normal speed, the I/O channel has the same speed as internal Bus: 4.77 MHz and one wait state for processor-generated I/O read/write cycles and 0 wait state for processor-generated memory read/write cycles. When the CPU is at turbo speed, instead of adding wait states, a slow bus speed is selected in 82C101 design to account for the slow I/O channel. The slow bus speed is either one half or one third of the system speed according to the value in bit 3 of system Configuration Register (Index 2). The 82C101 bus controller also generates enable signals and direction control signals for external buffers when the 8086 or the V30 CPU is used.

Bus Conversion

Since the 82C101 can operate with 16-bit processors (8086 or V30), a 16 bit multiplexed Data Bus is supported. A 16-bit processor read/write is converted to two 8-bit I/O channel read/write channels.

The 82C101 recognizes the need for Bus Conversion cycles when /BHE is low, A0 is low and any memory access to a location not in the planar RAM or ROM and I/O cycles to the locations are not internal to the 82C101.

Interrupt Controller

The Interrupt Controller is the functional equivalent of the 8259. It functions as an overall manager in an interrupt-driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests has a higher priority value than the level currently being serviced and issues an interrupt to the CPU based on this determination. It supports 8 maskable interrupt levels. Interrupt levels 2-7 are available at the system I/O channel. Interrupt levels 0 and 1 are generated internal to the 82C101. Level 0 is the highest priority and it is connected to counter/timer channel 0 to provide a periodical interrupt for the timer tick. Level 1 is used for the keyboard and is connected internally to the keyboard interface.

HARDWARE INTERRUPT ASSIGNMENT

Level	Usage
NMI	Parity Check IO CHCK Coprocessor
0	Timer
1	Keyboard
2	Reserved
3	Serial Port (Secondary)
4	Serial Port (Primary)
5	Hard Disk
6	Floppy Disk
7	Parallel Port

NMI

82C101 also handles nonmaskable interrupts coming from numeric coprocessor, parity checker and I/O channel check (/IOCHCK) signal. Since only one NMI pin exists on the processor, the NMI service routine reads a register (Port 62H) to determine the source of the NMI.

DMA Controller

The DMA Controller is functionally equivalent to the 8237 DMA Controller. It is designed to improve system performance by allowing external devices to directly transfer information between a peripheral device and system memory. The DMA controller supports single, block, demand and memory to memory transfer modes. It has 4 DMA channels, capable of Addr increment/decrement and masking of individual DMA request. Channel 0 is reserved for RAM memory refresh. Each DMA channel has a pair of 16-bit counters and a reloadable register for each counter. The 16-bit counters allow the DMA to transfer blocks as large as 64K bytes. The 8237 is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. State I (SI) is the inactive state. It is entered when the 8237 has no valid DMA requests pending. When in SI, the DMA Controller is inactive but may be in the program condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237 has requested a Hold but the processor has not yet returned an Acknowledge. The 8237 may still be programmed until it receives HLDA from the CPU. An Acknowledge from the CPU will signal that DMA Transfers may begin. S1, S2, S3, and S4 are the working states of the DMA service. If more time is needed to complete a transfer, Wait State (WS) can be inserted between S3 and S4 by the use of Ready line generated inside the 82C101.

Timer

The Timer circuit is functionally equivalent to the 8254 timer. Channel 0 is used as a general purpose software interrupt timer. Channel 1 is used for DRAM Refresh and Channel 2 is used to support tone generation for the audio speaker.

The Counter/Timer in the 82C101 solves one of the most common problems in any microcomputer system--the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and also programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated. The Counter/Timer contains 3 16-bit counters (counter 0-2) which can be programmed to count in binary or Binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

Programmable Peripheral Interface (PPI)

The 82C101 PPI is a subset of the 8255. It is limited to mode 0 (Basic input/output). No handshake is required when data is read from or written to a specific port. I/O Address 60H is referred to as Port A. 61H is Port B and 62H is Port C. Port 63H is the command/mode register for these three I/O ports. In the normal operation of the PC/XT, the control word is programmed to 99H: Port A (60H) and Port C (62H) are inputs, and Port B (61H) is output.

The input portion of Port A (60H) is for the keyboard scan code. Port B (61H) is the control port and Port C (62H) is the status port for various system configurations.

Parity Generator

The parity generator checks and generates even parity for RAM memory.

Keyboard Controller

The keyboard provides two keyboard interface signals, KBDATA and KBCLK. The interface logic assembles the serial data from the keyboard into bytes. Timing and synchronization is provided by the KBCLK signal. Internally there are shift registers clocked by KBCLK.

When a key is depressed or released, the keyboard controller sends a scan code. The keyboard logic assembles the incoming serial data to a byte. Whenever a byte of information is ready, an IRQ1 is sent to the interrupt controller. The IRQ1 interrupter service routine reads Port 60H to get the keyboard scan code and acknowledge by sending a positive pulse on Port 61H. This clears the shift register for the next incoming character.

Programming

The 82C101accepts I/O read/write commands from the CPU.

I/O Address Map

Address	Use
000-00F	DMA controller
020-021	Interrupt controller
040-043	Timer
060-063	PPI
081-083	DMA page registers
0A0	NMI mask register
100-1FF	Register

The timer is programmed like the 8254 timer. The DMA controller is programmed like the 8237 DMA controller, and the interrupt controller is programmed like the 8259 interrupt controller.

Keyboard Data Register

The Keyboard Data Register is a read only register to read data from the keyboard. When a character is in the register, Interrupt is sent to the Interrupt Controller, IRQ1 INPUT. The register can be cleared by setting Bit 7 of the PPI register.

Control Register (060H)

Data Bit	Use
0	Keyboard Scan Code
1	Keyboard Scan Code
2	Keyboard Scan Code
3	Keyboard Scan Code
4	Keyboard Scan Code
5	Keyboard Scan Code
6	Keyboard Scan Code
7	Keyboard Scan Code

Control Register (061H)

Data Bit	Use
0	Gate speaker timer channel
1	Gate speaker data
2	Switch register select
3	Not used
4	Disable parity check
5	Disable I/O check
6	Enable keyboard clock
7	Clear keyboard data register

Control Register (062H)

Data Bit	PB3 = LOW	PB3 = HIGH
0	Loop on POST	Display 0
1	+Coprocessor	Display 1 installed
2	+Planar RAM size 0	#5-1/4 drive 0
3	+Planar RAM size 1	#5-1/4 drive 1
4	Spare	Spare
5	+Timer channel 2 out	+Timer channel 2 out
6	+I/O channel check	+I/O channel check
7	+RAM parity check	+RAM parity chec

Command/Mode Register (063H)

	HEX 99
Mode Register Value	7 6 5 4 3 2 1 0
	1 0 0 1 1 0 0 1

Page Registers (081-083H)

The page registers are read/write registers to generate address bits 16-19 during a DMA transfer.

Address	Page Register
81	DMA Channel 2
82	DMA Channel 3
83	DMA Channel 1

Page Register

Data Bit	Use
0	Address bit 16
1	Address bit 17
2	Address bit 18
3	Address bit 19

NMI Mask Register (0A0H)

The NMI mask register enables the NMI to the CPU (8088).

Data Bit	Use
0-6	Not used
7	Enable NMI

Hardware Configuration Switches

The 82C101features a reset strap option. This option is to provide strap options without having to use pins. The 82C101 uses /DACKX lines to implement this feature. These pins are normally output, but they are used as inputs during power-up reset to select various configuration options. The following table describes the pins that are used in the strap option.

Pin	Strap Option
/DACK1	CPU (16 or 8 bit memory/IO) 0 - The 82C101 is used with an 8088 (or V20) processor. 1 - The 82C101 is used with an 8086 (or V30) processor.
/DACK2	CPU clock duty cycle 0 - 33% duty cycle (8086/88). 1 - 50% duty cycle (V20/V30).

Configuration Registers

There are 10 internal registers to define the 82C101 configuration. These registers are accessed through an indirect addressing scheme using I/O addresses F2 and F3. I/O address F2 contains the write-only configuration index register. I/O address F3 contains the writable/readable configuration data register.

Accessing the configuration registers is a two step process as follows:

Step 1: Write the index of the configuration register to I/O port F2.
Step 2: Followed by a read/write to I/O port F3.

To write a value of "AA" into configuration register 2. The index register at I/O address F2 must be written with a value of "2," then register at I/O address F3 with a value of "AA."

The configuration setup should be the first task performed after power is turned on, because, it defines how the 82C101 interfaces with the rest of the system. For example, it selects the memory size, and system timing. The functions of each configuration register are detailed below:

Index 0 -- DIP Switch Emulation

It is used to emulate the configuration DIP switches in an XT system. Default is 00H.

Bit	Function
7,6	Display type 00 EGA 01 CGA 40 x 25 10 CGA 80 x 25 01 Monochrome 80 x 25
5,4	Number of diskette drive installed 00 0 disk installed 01 1 disk installed 10 2 disk installed 11 3 disk installed
3	Loop on POST 0 No loop on POST 1 Loop on POST
2	Numeric processor installed 0 Not installed 1 Installed
1,0	Base RAM size 00 265KB 01 512KB 10 576KB 11 640KB

Index 1 -- Memory Configuration

It is used to select one of the 10 memory configurations from 256KB to 2944KB.

Bit	Function
3:0	Memory configuration (see the following table).

The first column is the value that should be set in the memory configuration register. The next 4 columns specify the type of device used for the respective bank. The next two columns specify the amount of base memory and EMS memory respectively. The last column indicates the total amount of memory.

Index 2 -- System configuration

Bit	Function
4	Clock frequency select 0 CPUCLK = 4.77MHz (non-turbo mode.) Default. 1 CPUCLK/3 = CLKIN/ (turbo mode.)
3	SYSCLK frequency AT turbo mode 0 SYSCLK = CPUCLK/3. Default. 1 SYSCLK = CPUCLK/2.
2	Slow CPUCLK frequency 0 CPUCLK frequency defined by Bit 4. Default. 1 CPUCLK = 4.77 MHz/2.
1	5-DRAM mode. 5 of 256Kx4 DRAMs for 640K memory. 0 Not 5-DRAM mode. Default. 1 5-DRAM mode.
0	Wait state for memory cycle when address range 0-640k is accessed in 5-DRAM mode. 0 No wait state. Default. 1 1 wait state.

*Bit 2 settings overrides Bit 4 settings.

Index 3 -- EMS

Bit	Function
2	EMS enable 0 EMS not enabled. Default. 1 EMS enabled.
1,0	Base address of EMS window. 00 C0000. Default 01 C8000. 10 D0000.

Index 4 -- EMS Page Register 0

Bit	Function
7	ER0, A21
6	ER0, A20
5	ER0, A19
4	ER0, A18
3	ER0, A17
2	ER0, A16
1	ER0, A15
0	ER0, A14

Index 5 -- EMS Page Register 1

Bit	Function
7	ER1, A21
6	ER1, A20
5	ER1, A19
4	ER1, A18
3	ER1, A17
2	ER1, A16
1	ER1, A15
0	ER1, A14

Index 6 -- EMS Page Register 2

Bit	Function
7	ER2, A21
6	ER2, A20
5	ER2, A19
4	ER2, A18
3	ER2, A17
2	ER2, A16
1	ER2, A15
0	ER2, A14

Index 7 -- EMS Page Register 3

Bit	Function
7	ER3, A21
6	ER3, A20
5	ER3, A19
4	ER3, A18
3	ER3, A17
2	ER3, A16
1	ER3, A15
0	ER3, A14

Index 8 -- Shadow RAM Enable

Bit	Function
5	Shadow RAM is enabled at location F0000-FFFFF. 0 Not enabled. Default. 1 Enabled.
4	Shadow RAM is enabled at location E0000-EFFFF. 0 Not enabled. Default. 1 Enabled.
3	Shadow RAM is enabled at location D8000-DFFFF. 0 Not enabled. Default. 1 Enabled.
2	Shadow RAM is enabled at location D0000-D7FFF. 0 Not enabled. Default. 1 Enabled.
1	Shadow RAM is enabled at location C8000-CFFFF. 0 Not enabled. Default. 1 Enabled.
0	Shadow RAM is enabled at location C0000-C7FFF. 0 Not enabled. Default. 1 Enabled.

Index 9 -- Shadow RAM write only

Bit	Function
5	Shadow RAM for F0000-FFFFF is in write mode. 0 Not in shadow write mode. Default. 1 In shadow write mode.
4	Shadow RAM for E0000-EFFFF is in write mode. 0 Not in shadow write mode. Default. 1 In shadow write mode.
3	Shadow RAM for D8000-DFFFF is in write mode. 0 Not in shadow write mode. Default. 1 In shadow write mode.
2	Shadow RAM for D0000-D7FFF is in write mode. 0 Not in shadow write mode. Default. 1 In shadow write mode.
1	Shadow RAM for C8000-CFFFF is in write mode. 0 Not in shadow write mode. Default. 1 In shadow write mode.
0	Shadow RAM for C0000-C7FFF is in write mode. 0 Not in shadow write mode. Default. 1 In shadow write mode.

DRAM Speed Selection Guide

	5 DRAM Configuration	No 5 DRAM Configuration
12 MHz		
10 MHz	100	150
4.77 MHz	150	150

Value	B0	B1	B2	B3	Base	EMS	Total
8088 (V20) configuration (non 5-DRAM)							
0	256K	--	--	--	256K	--	256K
1	256K	256K	--	--	512K	--	512K
2	256K	256K	256K	--	640K	128K	768K
3	256K	256K	256K	256K	640K	384K	1024K
4	256K	256K	256K	256K	512K	512K	1024K
5	1M	--	--	--	640K	384K	1024K
6	256K	1M	--	--	640K	640K	1280K
7	256K	256K	1M	--	640K	896K	1536K
8	1M	1M	--	--	640K	1408K	2048K
9	256K	1M	1M	--	640K	1664K	2304K
A	256K	256K	1M	1M	640K	1920K	2560K
8088 (V20) configuration (5-DRAM)							
0	640K	--	--	--	640K	--	640K
1	640K	256K	--	--	640K	256K	896K
2	640K	256K	256K	--	640K	512K	1152K
3	640K	256K	256K	256K	640K	768K	1408K
4	640K	256K	256K	256K	512K	896K	1408K
5	invalid						
6	640K	1M	--	--	640K	1024K	1664K
7	640K	256K	1M	--	640K	1280K	1920K
8	invalid						
9	640K	1M	1M	--	640K	2048K	2688K
A	640K	256K	1M	1M	640K	2304K	2944K
8086 (V30) configuration							
0	invalid						
1	256K	256K	--	--	512K	--	512K
2	invalid						
3	256K	256K	256K	256K	640K	384K	1024K
4	256K	256K	256K	256K	512K	512K	1024K
5	invalid						
6	invalid						
7	invalid						
8	1M	1M	--	--	640K	1408K	2048K
9	invalid						
A	256K	256K	1M	1M	640K	1920K	2560K

EMS 4.0

EMS (Expanded Memory Specification) is a method of indirectly addressing an extended area of RAM. EMS uses a window in the 384 KB address range dedicated to the system, and indirectly addresses memory through that window. There are four EMS registers in the 82C101.

The main application for EMS is in DOS systems whose programs can only access 1MB because the address range has only 20 address bits. (The 8086 had only 20 bits). If a system has more than 1 MB of RAM, and DOS can only address 1 MB, the remaining memory can only be used by addressing the memory indirectly.

The EMS window is broken into four 16-KB segments. Each of these segments is associated with one of four EMS address registers (see Figure 2), where each EMS address register represents eight address bits (A21 to A14). When the EMS window is selected, these bits replace system address bits A21 to A14, giving EMS software the ability to redirect memory addresses from the four EMS windows to anywhere in the resident RAM address range.

EMS is enabled in the Configuration Register by writing a one to Bit 2 of Register 33. The four EMS address registers are also programmed within the Configuration Registers.

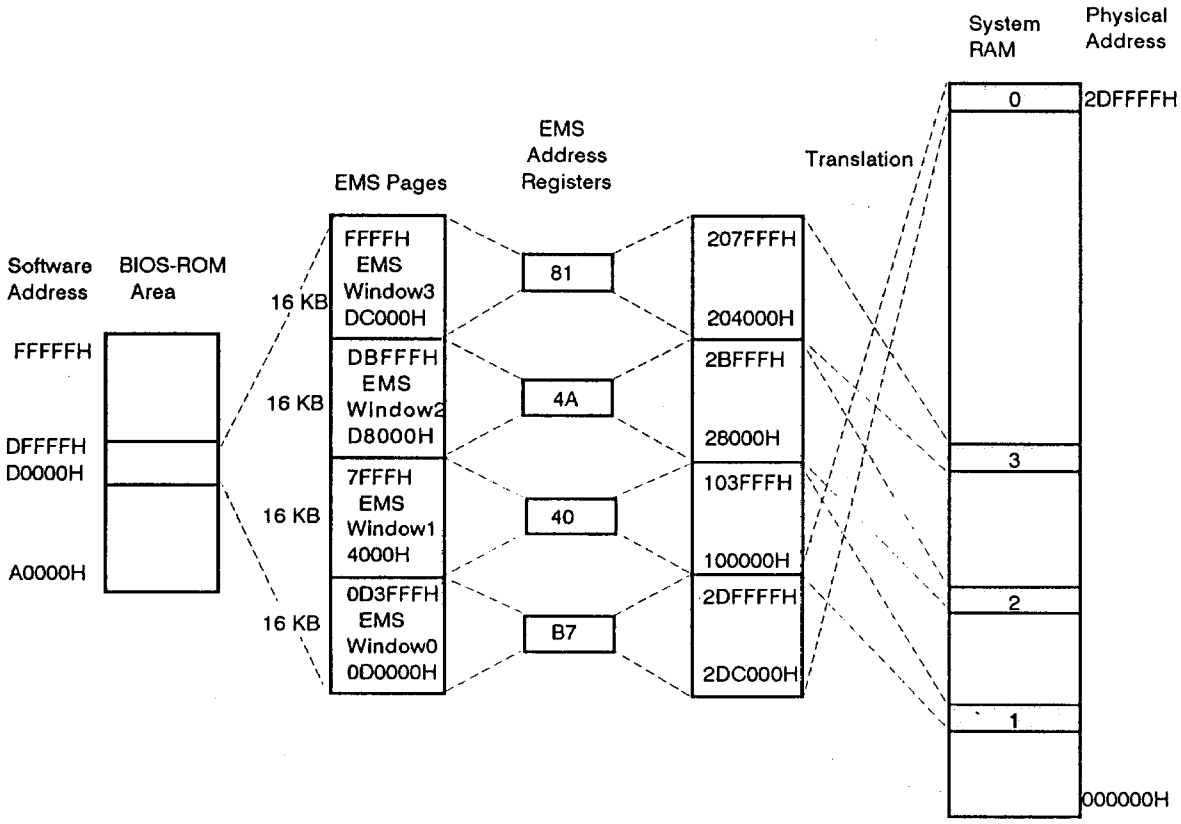


Figure 2 Memory Address Translation

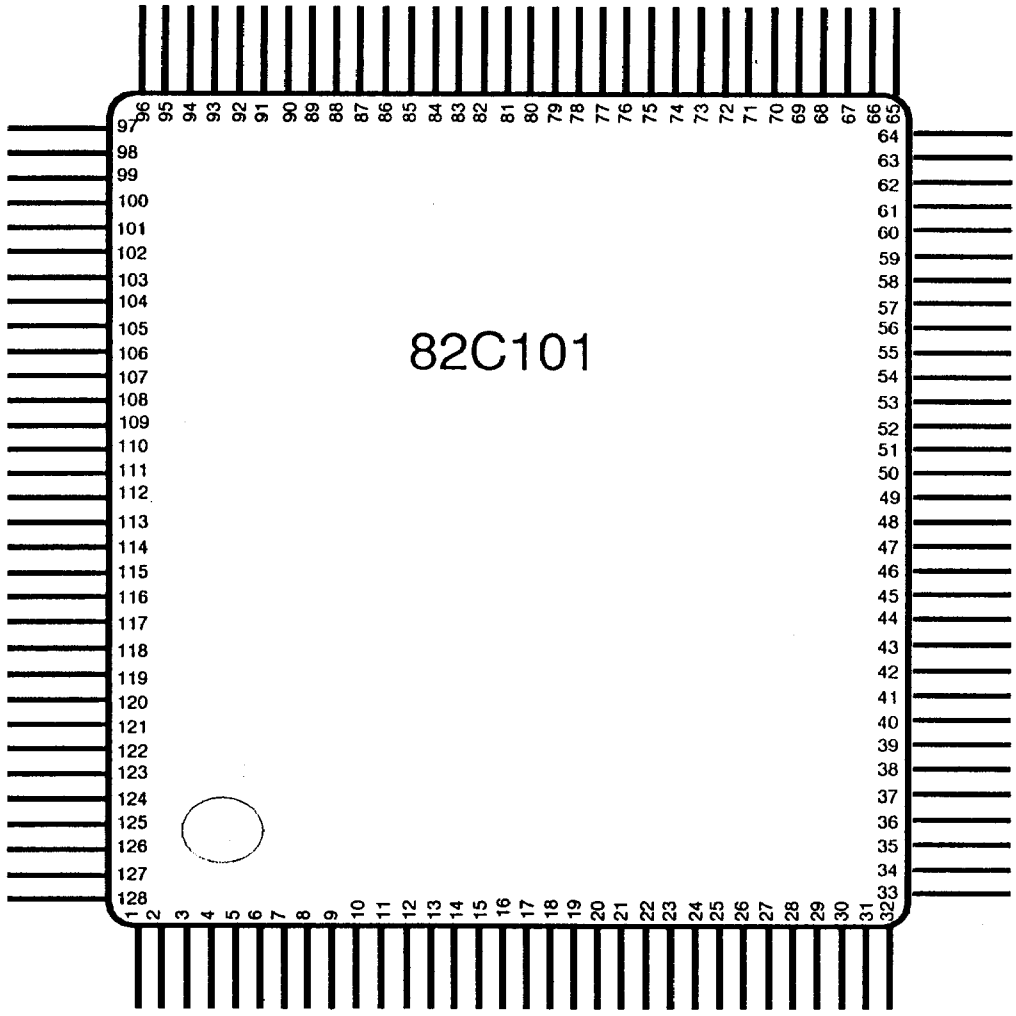
For example, to access memory at location 230FFF, EMS must be enabled and an address register must be programmed with 10-0011-00 and the 16 KB block of memory from 230000 to 233FFF is available for Register 0 (located between D0000 to D3FFF). A memory access to software address D0FFF is directed to 230FFF.

Shadow RAM

Shadow RAM provides an option to transfer BIOS or video-extension BIOS program codes into system RAM. This option provides significant performance improvement for applications requiring intensive BIOS calls.

Shadow RAM implements an alternate BIOS source by copying the complete EPROM program code into system RAM. This is referred to as "shadowing" because the DRAM and EPROM are both located at the same physical address space. This change is transparent to the rest of the system. ROM can be diabled, allowing the RAM to respond in its place. The advantage of this procedure is that DRAM access time is typically much faster than EPROM access time.
The 82C101 Shadow RAM is configured as 6 independent segments. Shadow RAM is implemented by using internal configuration registers 8 and 9. Enabling each Shadow RAM segment requires two steps. The "Shadow RAM Write Mode" is activated first to allow the transfer of code from EPROM to DRAM. Transfer is made by a read from the EPROM and a write to system DRAM at the same address. The next step activates the "Shadow RAM Enable" of the corresponding segment, disables the EPROM in that segment, and places the DRAM in that segment into read-only mode.

Pin Diagram



1 VSS	17 VCC	33 SD0	49 VCC	65 SD4	81 VSS	97 VSS	113 VCC
2 AD7 (SD15)	18 MD7	34 SD1	50 OSC	66 SD5	82 SA8	98 SA13	114 A16 (/BHE)
3 SA16	19 /IOR	35 SD2	51 IRQ2	67 SD6	83 SA9	99 SA14	115 A17 (PARH)
4 SA17	20 /IOW	36 SD3	52 IRQ3	68 SD7	84 SA10	100 SA15	116 A18 (DT/R)
5 SA18	21 PARL	37 KBCLK	53 IRQ4	69 SPKR	85 SA11	101 /CAS0	117 A19 (G646)
6 SA19	22 READY	38 DRQ1	54 IRQ5	70 /IOCHCK	86 ALE	102 /CAS1	118 MA0
7 MA7	23 /MEMR	39 DRQ2	55 IRQ6	71 CLKIN	87 CPUCLK	103 /CAS2 (C646)	119 MA1
8 MA8	24 /MEMW	40 DRQ3	56 IRQ7	72 /DACK0	88 /LOCK	104 /CAS3 (/G245)	120 MA2
9 MA9	25 /RAS0	41 RESET	57 IOCHRDY	73 /DACK1	89 /S0	105 A8 (MD8)	121 MA3
10 MD0	26 /RAS1	42 /RESET	58 SYSCLK	74 /DACK2	90 /S1	106 A9 (MD9)	122 MA4
11 MD1	27 A0	43 /INT87	59 KBDATA	75 /DACK3	91/S2	107 A10 (MD10)	123 MA5
12 MD2	28 SA0	44 SALE	60 SA4	76 PWRGD	92 AD0 (SD8)	108 A11 (MD11)	124 MA6
13 MD3	29 SA1	45 NMI	61 SA5	77 TC	93 AD1 (SD9)	109 A12 (MD12)	125 /WE
14 MD4	30 SA2	46 INTR	62 SA6	78 VCC	94 AD2 (SD10)	110 A13 (MD13)	126 AD4 (SD12)
15 MD5	31 SA3	47 /ROMCS	63 SA7	79 X14MI	95 AD3 (SD11)	111 A14 (MD14)	127 AD5 (SD13)
16 MD6	32 VSS	48 AEN	64 VSS	80 X14MO	96 SA12	112 A15 (MD15)	128 AD6 (SD14)

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
X14MI	79	I		14.318 MHz crystal input.
X14MO	80	O		14.318 MHz crystal output.
CLKIN	71	I		Optional oscillator input for turbo clock.
CPUCLK	87	O		Clock for the CPU.
SYSCLK	58	O		Clock for the peripherals.
OSC	50	O		14.318 MHz oscillator output.
RESET	41	O		System reset. Active high.
/RESET	42	O		System reset. Active low.
PWRGD	76	I		"Power good" indicator from the power supply, when low, a power-up reset is generated.
/S0	89	I		CPU Status.
/S1	90	I		
/S2	91	I		
READY	22	O		Ready signal to the CPU.
/LOCK	88	I		When low, system bus is locked by CPU.
ALE	86	O		Address latch enable.
SALE	44	O		System address latch enable.
AD0 (SD8)	92	I/O	88 86	CPU multiplexed address data bus bit 0. System data bus bit 8.
AD1 (SD9)	93	I/O	88 86	CPU multiplexed address data bus bit 1. System data bus bit 9.
AD2 (SD10)	94	I/O	88 86	CPU multiplexed address data bus bit 2. System data bus bit 10.

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
AD3 (SD11)	95	I/O	88 86	CPU multiplexed address data bus bit 3. System data bus bit 11.
AD4 (SD12)	126	I/O	88 86	CPU multiplexed address data bus bit 4. System data bus bit 12.
AD5 (SD13)	127	I/O	88 86	CPU multiplexed address data bus bit 5. System data bus bit 13.
AD6 (SD14)	128	I/O	88 86	CPU multiplexed address data bus bit 6. System data bus bit 14.
AD7 (SD15)	2	I/O	88 86	CPU multiplexed address data bus bit 7. System data bus bit 15.
A8 (MD8)	105	I/O	88 86	CPU address bus bit 8. DRAM data bus bit 8.
A9 (MD9)	106	I/O	88 86	CPU address bus bit 9. DRAM data bus bit 9.
A10 (MD10)	107	I/O	88 86	CPU address bus bit 10. DRAM data bus bit 10.
A11 (MD11)	108	I/O	88 86	CPU address bus bit 11. DRAM data bus bit 11.
A12 (MD12)	109	I/O	88 86	CPU address bus bit 12. DRAM data bus bit 12.
A13 (MD13)	110	I/O	88 86	CPU address bus bit 13. DRAM data bus bit 13.
A14 (MD14)	111	I/O	88 86	CPU address bus bit 14. DRAM data bus bit 14.
A15 (MD15)	112	I/O	88 86	CPU address bus bit 15. DRAM data bus bit 15.

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
A16 (/BHE)	114	I	88 86	CPU address bus bit 16. Bus high enable. /BHE and SA0 indicate the type of bus transfer. /BHE SA0 Type 0 0 16 bit transfer 0 1 odd byte transfer 1 0 even byte transfer 1 1 invalid
A17 (PARH)	115	I/O	88 86	CPU address bus bit 17. Parity bit from the high byte of the DRAMs.
A18 (DT/R)	116	I/O	88 86	CPU address bus bit 18. Direction control of data flow through the transceivers between 82C101 and CPU.
A19 (G646)	117	I/O	88 86	CPU address bus bit 19. Enable signal of the data transceiver (646) which controls the data flow between CPU low byte data bus and 82C101.
SA0	28	O		System address bus bit 0.
SA1	29	I/O		System address bus bit 1.
SA2	30	I/O		System address bus bit 2.
SA3	31	I/O		System address bus bit 3.
SA4	60	I/O		System address bus bit 4.
SA5	61	I/O		System address bus bit 5.
SA6	62	I/O		System address bus bit 6.
SA7	63	I/O		System address bus bit 7.
SA8	82	I/O		System address bus bit 8.

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
SA9	83	I/O		System address bus bit 9.
SA10	84	I/O		System address bus bit 10.
SA11	85	I/O		System address bus bit 11.
SA12	96	I/O		System address bus bit 12.
SA13	98	I/O		System address bus bit 13.
SA14	99	I/O		System address bus bit 14.
SA15	100	I/O		System address bus bit 15.
SA16	3	I/O		System address bus bit 16.
SA17	4	I/O		System address bus bit 17.
SA18	5	I/O		System address bus bit 18.
SA19	6	I/O		System address bus bit 19.
A0	27	I		CPU address bus bit 0. Used in Mode 86 only.
/MEMR	23	O		Memory read command.
/MEMW	24	O		Memory write command.
/IOR	19	O		I/O read command.
/IOW	20	O		I/O write command.
SD0	33	I/O		System data bus bit 0.
SD1	34	I/O		System data bus bit 1.
SD2	35	I/O		System data bus bit 2.

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
SD3	36	I/O		System data bus bit 3.
SD4	65	I/O		System data bus bit 4.
SD5	66	I/O		System data bus bit 5.
SD6	67	I/O		System data bus bit 6.
SD7	68	I/O		System data bus bit 7.
/IOCHCK	70	I		When low, it indicates there is a parity or other error from memory or devices on the I/O channel.
IOCHRDY	57	I		I/O channel ready.
AEN	48	O		System address enable. When high, indicates that the DMA controller has control of the the address bus, data bus and the appropriate command lines.
DRQ1	38	I		DMA request line for channel 1.
DRQ2	39	I		DMA request line for channel 2.
DRQ3	40	I		DMA request line for channel 3.
/DACK0	72	O		DMA acknowledge for channel 0. When low, indicates a refresh cycle.
/DACK1	73	I/O		DMA acknowledge for channel 1.
/DACK2	74	I/O		DMA acknowledge for channel 2.
/DACK3	75	O		DMA acknowledge for channel 3.
TC	77	O		When high, indicates the terminal count of any DMA channel is reached.
/ROMCS	47	O		ROM chip select. Top 64k decode (F0000 - FFFFF).

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
MA0	118	O		Multiplexed DRAM address bit 0.
MA1	119	O		Multiplexed DRAM address bit 1.
MA2	120	O		Multiplexed DRAM address bit 2.
MA3	121	O		Multiplexed DRAM address bit 3.
MA4	122	O		Multiplexed DRAM address bit 4.
MA5	123	O		Multiplexed DRAM address bit 5.
MA6	124	O		Multiplexed DRAM address bit 6.
MA7	7	O		Multiplexed DRAM address bit 7.
MA8	8	O		Multiplexed DRAM address bit 8.
MA9	9	O		Multiplexed DRAM address bit 9.
MD0	10	I/O		DRAM data bus bit 0.
MD1	11	I/O		DRAM data bus bit 1.
MD2	12	I/O		DRAM data bus bit 2.
MD3	13	I/O		DRAM data bus bit 3.
MD4	14	I/O		DRAM data bus bit 4.
MD5	15	I/O		DRAM data bus bit 5.
MD6	16	I/O		DRAM data bus bit 6.
MD7	18	I/O		DRAM data bus bit 7.
PARL	21	I/O		Parity bit from the low byte of the DRAMs.
/RAS0	25	O		Row address strobe for DRAM.
/RAS1	26	O		Row address strobe for DRAM.

Pin Descriptions

Symbol	Pin	I/O	Mode	Pin Description
/CAS0	101	O		Column address strobe for DRAM.
/CAS1	102	O		Column address strobe for DRAM.
/CAS2 (C646)	103	O	88 86	Column address strobe for DRAM. Clock for the external buffer 646.
/CAS3 (/G245)	104	O	88 86	Column address strobe for DRAM. Enable signal of the data transceiver (245) which controls the data flow between CPU high byte data bus and 82C101.
/WE	125	O		DRAM write enable.
/INT87	43	I		Unmasked exception during numeric instruction execution when 8087 coprocessor interrupt is enabled.
IRQ2	51	I		Interrupt request line 2.
IRQ3	52	I		Interrupt request line 3.
IRQ4	53	I		Interrupt request line 4.
IRQ5	54	I		Interrupt request line 5.
IRQ6	55	I		Interrupt request line 6.
IRQ7	56	I		Interrupt request line 7.
INTR	46	O		Interrupt request to the CPU.
NMI	45	O		Non-maskable interrupt to the CPU.
SPKR	69	O		Speaker output.
KBCLK	37	I/O		Keyboard clock.
KBDATA	59	I/O		Keyboard data.
VCC	78,113,17,49			
VSS	81,97,32,64,1			

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Units
Power supply voltage	VDD	-0.5	7.0	V
Input, Output voltage	Vin Vout	-0.5 to VDD	+0.5	V
DC Current Drain per Pin any input or output**	I		25	uA
DC Current Drain VDD and VCC Pins	I		100	uA
Storage Temperature	Tstg	-55	150	°C
Lead Temperature less than 10sec. solder	Tl		250	°C
Operating Temperature Commercial	Toper	0	70	°C

* Exposing the device to stresses above those listed can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

** Except 48 mA output pads which have a limit of 48mA.

Capacitance

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at
Output Capacitance	CO		10	pF	
I/O Capacitance	CIO		10	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 10%

/S0, /S1, /S2, /LOCK, A16 (/BHE), X14MI

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC

/INT87, /IOCHCK, IOCHRDY, DRQ1, DRQ2, DRQ3, IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL	-60	-175	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = 5.5V

PWRGD

Parameter	Symbol	Min	Max	Unit	Test Condition
Threshold voltage low to high	VTHL	2.3	3.1	V	VCC = 5 +/- 0.5 V
Threshold voltage high to low	VTHL	1.7	2.3	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = 5.5V

NMI, ALE, /ROMCS, INTR, CPUCLK, READY, /DACK0, /DACK3, X14M2

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL=4.0mA VCC=4.5V
Output high voltage	VOH	2.4		V	IOH=-8.0mA VCC=4.5V

MA0-9, /WE, /RAS0-1, /CAS0-3

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 8.0mA VCC=4.5V
Output high voltage	VOH	2.4		V	IOH = -8.0mA VCC=4.5

AEN, SALE, RESET, /RESET, OSC, TC, SA0, /IRR, /IOW, SYSCLK

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL=16.0mA VCC=4.5V
Output high voltage	VOH	2.4		V	IOH=-16.0mA VCC=4.5V

MD0-7, A8 (MD8), A9 (MD9), A10 (MD10), A11 (MD11), A12 (MDR), A13 (BD13), A14 (MD14), A15 (MD15), A17 (PARH), A18 (DT/R), A19 (G646), PARL, /DACK1, /DACK2

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 4.0mA
Output high voltage	VOH	2.4			IOH = -4.0mA
Output impedance	IOZ	-10.0	10.0	uV	0V<VOUT<5.5V

SD0-7, AD0 (SD8), AD1 (SD9), AD2 (SD10), AD3 (SD11), AD4 (SD12), AD5 (SD13), AD6 (SD14), AD7 (SD15), KBCLK, KBDATA

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 16mA
Output high voltage	VOH	2.4			IOH = -16.0mA
Output impedance	IOZ	-10.0	10.0	uV	0V<VOUT<5.5V

/MEMR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 16mA
Output high voltage	VOH	2.4			IOH = -16mA
Output impedance	IOZ	-10.0	175	uV	0V<VOUT<5.5

SPKR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 16mA