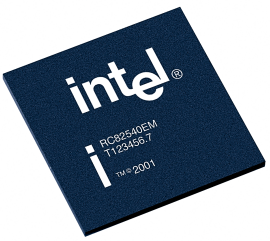

Intel® 82540EM Gigabit Ethernet Controller

High-Performance Gigabit Connection for Desktop Designs

Product Brief

The Intelligent Way to Connect

- Footprint compatibility allows for flexible designs
- Lower system costs and higher density
- ASF 1.0 and SMBus 2.0 enabled

Product Description

The Intel® 82540EM Gigabit Ethernet Controller integrates Gigabit Ethernet MAC and PHY layer functions in a single, compact component. Packaged in a 15x15mm TFBGA, the Intel 82540EM Gigabit Ethernet Controller is physically and electrically compatible with the Intel® 82551QM and 88551ER Fast Ethernet Controllers, allowing for a flexible, Gigabit Ethernet or 10/100 Ethernet design.

The Intel 82540EM combines Intel's fourth-generation Gigabit MAC design, with fully integrated, physical-layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, 802.3ab). In addition, the controller provides a direct Peripheral Component Interconnect (PCI) 2.2 compliant bus up to 66MHz.

The Intel 82540EM's on-board SMBus port enables enhanced manageability and system health monitoring via the LAN: Management packets can be routed to or from a management processor. The SMBus port enables implementation of industry standards such as IPMI (Intelligent Platform Management Interface). In addition, ASF 1.0 (Alert Standard Format) circuitry provides alerting and remote-control capabilities with standardized interfaces.

The Intel 82540EM Gigabit Ethernet Controller architecture is optimized to deliver both high-performance networking and PCI bus efficiency with the lowest power and smallest size. Using state logic design with a pipelined DMA Unit and 128-bit-wide buses for the fastest performance, the 82540EM controller handles Gigabit Ethernet traffic with low network latency and minimal internal processing overhead. The controller's architecture includes independent transmit and receive queues to limit PCI bus traffic, and a PCI interface that maximizes the use of bursts for efficient bus usage. The Intel 82540EM Gigabit Ethernet Controller prefetches up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage. A 64KB, on-chip packet buffer maintains superior performance as available PCI bandwidth changes. Advanced interrupt moderation hardware manages interrupts generated by the 82540EM controller to further improve system efficiency. In addition, using hardware acceleration, the controller also offloads tasks from the host processor, such as TCP/UDP/IP checksum calculations and TCP segmentation.

Applications

The Intel® 82540EM Gigabit Ethernet Controller is designed for use in the following applications:

- LAN on Motherboard (LOM) in desktop, mobile and other space-constrained designs
- Communications and networking devices requiring improved performance over 10/100 Ethernet
- Gigabit Ethernet connectivity for embedded clients such as Web kiosks and POS terminals

Features	Benefits
PCI Bus Features	
■ PCI revision 2.2, 32-bit, 33/66MHz	■ Application flexibility in LOM or embedded use
MAC Specific Features	
■ 64KB configurable RX and TX packet FIFO	■ No external FIFO memory requirements ■ FIFO size tunable to the application
■ Low-latency transmit and receive queues	■ Network packets handled without waiting or buffer overflow
■ IEEE 802.3x-compliant flow-control support with software-controllable	■ Reduced frame loss due to receive FIFO overrun
■ Caches up to 64 packet descriptors in a single burst	■ Efficient PCI-bandwidth usage
■ Programmable host memory receive buffers (256B to 16KB); Programmable cache line size from 16B to 256B	■ Efficient usage of PCI bandwidth
Gigabit PHY Specific Features	
■ Integrated PHYs for 10/100/1000Mb/s full- and half-duplex operation	■ Reduced board space and lower power dissipation
■ IEEE 802.3ab Auto-Negotiation	■ Automatic link configuration including speed, duplex, and flow control
■ Proven PHY compatible with IEEE 802.3ab	■ Robust operation over the installed base of CAT-5 twisted-pair cabling at lengths greater than 100m
■ State-of-the-art DSP architecture implements digital adaptive equalization, echo, cross-talk and baseline wander cancellation	■ Robust 1000Mb/s performance in noisy environments and despite severe cable installation problems
■ PHY detects polarity, MDI-X, 2 pair vs. 4 pair cables, and cable length	■ Easier network installation and maintenance
Host Offloading Features	
■ Transmit TCP segmentation IP, TCP, and UDP checksum off-loading capabilities on RX and TX	■ Increased throughput and lower CPU utilization. Compatible with large send offload feature found in Windows* 2000 and Windows* XP
■ Advanced packet filtering	■ 16 exact matched (unicast or multicast) ■ Promiscuous (unicast/multicast) transfer mode
■ IEEE 802.1Q VLAN support with VLAN tag insertion and stripping and packet filtering for up to 4096 VLAN tags	■ Enables IT staff to easily create multiple virtual LAN segments
■ Descriptor ring management hardware for TX and RX	■ Optimized fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
■ Jumbo frame support up to 16KB	■ High throughput for large data transfers on networks supporting jumbo frames
■ Interrupt moderation controls	■ Reduces the number of interrupts generated by receive and transmit operations
Manageability Features	
■ On-chip SMBus 2.0 port	■ Enables IPMI, and ASF implementations
■ ASF 1.0 alerting	■ Provides alerting and remote-control capabilities with standardized interfaces
■ Compliance with PCI Power Management v1.1/ACPI v2.0	■ PCI power management capability requirements for PC and embedded applications
■ Wake on LAN (WoL) support	■ Packet recognition and wakeup for network adapter and LOM applications without software configuration
■ Automatic link speed switching from 1000Mb/s down to 10 or 100Mb/s in standby	■ Low power in standby states ■ Supports power-down states without software assistance
■ Smart Power Down mode when no signal is detected on the wire	■ Enables very low power mobile or battery powered implementations
Additional Device Features	
■ Four programmable LED outputs	■ Indications for link speed, activity, duplex, collisions, pause by flow control, PCI speed, PCI width, and port ID on each port ■ Allows design customization without affecting software drivers
■ Internal PLL for clock generation using a 25MHz crystal or a 25MHz oscillator	■ Lower component count and cost
■ On-chip power regulator control circuitry	■ Fewer on-board power supply regulators ■ Simplified power supply design

Characteristics

Electrical

■ PCI Signaling	3.3V and 5V
■ Power Dissipation	1.8W (typical)

Environmental

■ Operating temperature	0°C to 70°C (maximum); Does not require a heat sink or forced airflow.
■ Storage temperature	-65°C to 140°C

Physical

■ Package	196-pin TFBGA, 1mm ball pitch, 15 X 15mm (Simplifies LOM board designs).
■ Footprint-compatible with Intel® 82551QM and 82551ER Fast Ethernet Controllers	Enables a Gigabit Ethernet or 10/100 LOM implementation on the same board.

For more information, contact your Intel® sales representative.

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