Intel® 82801EB (ICH5), 82801ER (ICH5R), 82801DB (ICH4), 82801CA (ICH3), 82801BA (ICH2), 82801AA (ICH), and 82801AB (ICH0) IDE Controller

Programmer's Reference Manual (PRM)

May 2003

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Contents

Tables

Revision History

Revision	Description	Date
-001	• Initial Release	November 2001
-002	• Added ICH4 (Intel® 82801DB Chipset) support	May 2002
-003	• Added ICH5 (Intel® 82801EB Chipset) and ICH5R (Intel® 82801ER Chipset) support	April 2003
-004	• Minor edits; some references to ICH 5 were inadvertently omitted in prior revision..	May 2003

1 Introduction

1.1 Overview

This document assists Independent Hardware Vendors (IHV) in supporting the feature set of the Intel® 8XX I/O Controller Hub (ICH) IDE Controller. General requirements for developing an IDE mini-port driver that utilizes the IDE Interface are described. The information in this document supplements the information provided in the Intel® 82801EB (ICH5), Intel® 82801ER (ICH5R), Intel® 82801DB (ICH4), Intel® 82801CA (ICH3), Intel® 82801BA (ICH2), the Intel® 82801AA (ICH), and the Intel® 82801AB (ICH0) I/O Controller Hub Datasheets, and is intended for IHVs and Intel customers developing their own driver interface.

Functions that BIOS or operating systems (OS) must perform to ensure correct and reliable operation of the platform are described. Software specifications for the IDE controller, including register information, are outlined. Details regarding the development of an IDE-based driver that is baseline for a production driver already in the marketplace are provided.

It is assumed that the reader has a working knowledge of the IDE architecture and the Intel® ICHx IDE controller implementation of the IDE specification. Also, the reader should understand the development of IDE drivers for the target operating system, including how to program to specific registers.

This document will be supplemented from time to time with specification updates that will contain information relating to the latest controller or programming changes. Check with your Intel representative for the availability of specification updates.

In addition, system software requirements for initializing the 82801EB (ICH5), 82801DB (ICH4), 82801CA (ICH3), 82801BA (ICH2), 82801AA (ICH), and 82801AB (ICH0) ATA Controllers (also known as Bus Master IDE Controllers) are discussed. These recommendations allow for the optimal operation of the ICH5, ICH4, ICH3, ICH2, ICH, and ICH0 ATA interface with the BIOS Disk Services and operating system ATA device drivers.

The recommendations in this Programmers Reference Manual (PRM) apply to the following components:

Table 1. Intel® ICH Device IDs

Device	Device Function Number	PCI Device ID	PCI Vendor ID
82801AA (ICH) ATA Controller	01h	2411h	8086h
82801AB (ICH0) ATA Controller	01h	2421h	8086h
82801BA (ICH2) & 82801BAM (ICH2-M) ATA Controller	01h	244Ah (Mobile, ATA/100) 244Bh (High-End, ATA/100)	8086h
82801CA (ICH3-S) & 82801CAM (ICH3-M) ATA Controller	01h	248Ah (Mobile, ATA/100) 248Bh (High-End, ATA/100)	8086h
82801DB (ICH4) & 82801DBM (ICH4-M) ATA Controller	01h	24CAh (Mobile, ATA/100) 24CBh (High-End, ATA/100)	8086h
82801EB (ICH5) & 82801ER (ICH5R) ATA Controller	01h	24DBh (High-End, ATA/100)	8086h

Note: **In this document, PIIX4 refers to both the 82371AB (PIIX4) and 82371EB (PIIX4E) devices. Also, "ICH Family" refers to the ICH5, ICH4, ICH3, ICH2, ICH, and ICH0 devices. Any reference to an ICHx device that has a corresponding ICHx-M device will include the ICHx-M part (i.e. reference to ICH2 includes the ICH2-M, reference to ICH3 includes ICH3-S and ICH3-M, reference to ICH4 includes ICH4-M, reference to ICH5 includes ICH5R).**

1.2 References

Table 2. Reference Documents and Information Sources

Document Name	Source
AT Attachment with Packet Interface – 6 (ATA/ATAPI-6), Document 1410D, Rev. 2	Technical Committee T13
AT Attachment with Packet Interface – 5 (ATA/ATAPI-5), Document 1321D, Rev. 3	Technical Committee T13
ATA Packet Interface for CD-ROMs, Rev 2.6	Small Form Factor Committee
ATAPI Removable Rewriteable Media Specification (INF-8070i)	Small Form Factor Committee
Programming Interface for Bus Master IDE Controller (SFF 8038i)	Small Form Factor Committee
82801AA/AB/BA/BAM/CA/CAM/DB/DBM/EB Datasheets	http://developer.intel.com/design/chipsets/datashts/index.htm
PCI Local Bus Specification, Revision 2.3	http://www.pcisig.com/home

2 Intel® ICH ATA Controller(s), Basic Attributes

The ICH family supports a dual controller architecture, of which a maximum of two ATA/ATAPI devices may be attached to each independent controller. A total of four devices are supported when both controllers are enabled. Each controller is considered a legacy PCI device, with a PCI configuration space that indicates dual legacy, non plug-and-play ATA devices. The term "Legacy" is also referred to as "Compatibility" mode/state in this document.

Note however, the new ICH5, ICH4, and ICH3 device may be programmed as a non-legacy or "Native" PCI device, with a PCI configuration space that indicates dual native plug-and-play ATA devices in addition to the default (reset) condition of a legacy PCI device.

There are two basic operating modes with respect to Data Transfers that are supported by the ICH ATA controller:

1. PIO: data is transferred between drive and host controller via Programmed I/O (PIO) cycles.

2. DMA: data is transferred between drive and host controller via DMA-based protocol.

There are two general classes of DMA-based drives: Ultra DMA and DMA drives (which include multi-word and single-word DMA). Note that the Ultra DMA protocol corresponds to the Ultra ATA/100, Ultra ATA/66, or Ultra ATA/33 specifications.

The ICH5 is new to this PRM. This new device, the ICH4, and the ICH3 device support native plug-and-play PCI operation. Building upon ICH2, the ICH5, ICH4 and ICH3 also include Ultra ATA/100 operation that increases the data transfer bandwidth of the ATA/ATAPI interface between host and device to 100MB/s. The Ultra ATA/100 specification is an extension of Ultra ATA/66 and Ultra ATA/33 specifications, where Ultra ATA/100 refers to the Ultra DMA 100 protocol, Ultra ATA/66 refers to the Ultra DMA 66 protocol and Ultra ATA/33 refers to the Ultra DMA 33 protocol.

Table 3. Transfer Modes Supported by the Intel® ICH5, ICH4, ICH3, ICH2, ICH, or ICH0 ATA Controller(s)

PIO Operating Mode	DMA Operating Mode	Effective Minimum Cycle Time	Intel® ICH2, ICH, or ICH0 Support
PIO0/PIO1/Compatible		900 ns	All
PIO2	Single-Word DMA Mode 2[1]	240 ns	All
PIO3 (with IORDY Flow Control)[2]	Multi-Word DMA Mode 1	180 ns	All
PIO4 (with IORDY Flow Control)[2]	Multi-Word DMA Mode 2, or Ultra DMA (ATA/33) Mode 0	120 ns	All
	Ultra DMA (ATA/33) Mode 1	80 ns	All
	Ultra DMA (ATA/33) Mode 2	60 ns	All
	Ultra DMA (ATA/66) Mode 3	45 ns	ICH, ICH2, ICH3, ICH4, or ICH5
	Ultra DMA (ATA/66) Mode 4	30 ns	ICH, ICH2, ICH3, ICH4, or ICH5
	Ultra DMA (ATA/100) Mode 5[3]	20 ns	ICH2, ICH3, ICH4, or ICH5

NOTES:
1. Single-Word DMA Mode 2 has been rendered Reserved/Obsolete in X3T13's ATA3 specification.
2. PIO3, PIO4 timings assume the use of the IORDY Flow Control to achieve the target cycle time.
3. Ultra DMA mode 5 is available on ICH2 (244B), ICH2M (244A), ICH3M (248A), ICH3S (248B), ICH4, and ICH5.

Each of the controllers on the ICH ATA controller(s) can be enabled independently. When the appropriate controller (Primary or Secondary) is enabled, or ICH5, ICH4 or ICH3 are enabled in their default compatibility (legacy) operating mode, the following resources are occupied:

Table 4. "Compatibility" (Legacy) Resource Usage

Resource Name	Resource Range and Type
Primary Controller's Command Block	I/O 1F0-1F7 (8 bytes)
Primary Controller's Control Block	I/O 3F6h (1byte)
Primary Controller's Bus-Master IDE Control Block	I/O 0xxx0-0xxx7h (8 bytes), where 0xxx0h is the value programmed in the "Bus Master IDE Base Address Register"
Primary Controller's Interrupt	IRQ 14 (ISA)
Secondary Controller's Command Block	I/O 170-177 (8 bytes)
Secondary Controller's Control Block	I/O 376h (1 byte)
Secondary Controller's Bus-Master IDE Control Block	I/O 0xxx8-0xxxFh (8 bytes), where 0xxx0h is the value programmed in the "Bus Master IDE Base Address Register"
Secondary Controller's Interrupt	IRQ 15 (ISA)

When the ICH5, ICH4 or ICH3 ATA controller(s) (Primary or Secondary) are enabled in its native PCI operating mode, the following resources are occupied:

Table 5"Native PCI" Resource Usage

Resource Name	Resource Range and Type
Primary Controller's Command Block	I/O 0xXXX0-0xXXX7h (8 bytes) where 0xxx0h is the value programmed in the "Primary Command Block Base Address Register"
Primary Controller's Control Block	I/O 0xXXX0-0xXXX3h (4 bytes) where 0xxx0h is the value programmed in the "Primary Control Block Base Address Register"
Primary Controller's Bus-Master IDE Control Block	I/O 0xxx0-0xxx7h (8 bytes), where 0xxx0h is the value programmed in the "Bus Master IDE Base Address Register"
Primary Controller's Interrupt	INT A-D (PCI)
Secondary Controller's Command Block	I/O 0xXXX0-0xXXX7h (8 bytes) where 0xxx0h is the value programmed in the "Primary Command Block Base Address Register"
Secondary Controller's Control Block	I/O 0xXXX0-0xXXX3h (4 bytes) where 0xxx0h is the value programmed in the "Primary Control Block Base Address Register"
Secondary Controller's Bus-Master IDE Control Block	I/O 0xxx8-0xxxFh (8 bytes), where 0xxx0h is the value programmed in the "Bus Master IDE Base Address Register"
Secondary Controller's Interrupt	INT A-D (PCI)

Additionally, the ICH5, ICH4 and ICH3 have one extra base address register with the following allocation requirements:

Table 6. Intel® ICH5, ICH4 and ICH3 Additional Resource Usage

Resource Name	Resource Range and Type
Reserved Control Block	Memory 0–3ffh (1 Kbyte)

Tips:

- When ICH5, ICH4 or ICH3 are programmed in the "native" PCI configuration, the system still consumes IRQ14 and 15 due to the method of routing the ATA interrupts on the board.
- All resources (I/O, Memory or Interrupt) that are controlled by either a Base Address Register (BAR) or an Interrupt Level/Pin register in the PCI configuration space for this device are determined at boot by the PCI enumeration process
- All valid BARs must be initialized according to the method prescribed in the *PCI Local Bus Specification, Revision 2.3*. Any BARs that are not initialized will prevent proper operation of the ATA controller. Note that ICH5, ICH4 and ICH3 have six BARs that must be filled out and the first four are option based on whether the controller is programmed in compatibility or native mode.

The "ICH family" ATA controller corresponds to Function 1 on each of the ICH family components. In order to interface with a Plug and Play Operating System when the above requirements are fulfilled, no additional Plug and Play device node resource allocation is necessary for the ICH ATA device.

3 Software Initialization Requirements

The ICH devices are functionally backwards compatible with the PIIX4 ATA Controllers. This document will address all programming of the PIIX4 ATA Controller, but will specifically point out the incremental programming for the ICH devices, calling out specific details between ICH5, ICH4, ICH3, ICH2, ICH, and ICH0 where applicable. System software that initializes the Intel Ultra ATA Controller should ensure that the following steps have taken place:

1. For ICH5, ICH4 and ICH3, enable "Compatibility" or "Native PCI" operation as desired.
    a) If Compatibility operation is selected, then continue to Step #2.
    b) If Native PCI is selected, complete the following:
        i. Enable Native operation in the Programming Interface register (ICH5, ICH4 and ICH3: Function 1 PCI Config. Offset 9h)
        ii. Task-File (Command and Control) I/O BAR0-3 (ICH Function 1 PCI Config. Offset 10-1Fh) have each been assigned to a 16-bit Base I/O Address.
2. Enable Expansion (ICH5, ICH4 and ICH3) controller memory configuration:
    a) PCI "Expansion Base Memory Address" register (ICH Function 1 PCI Config. Offset 24–27h) has been assigned to a 32-bit Base Memory Address that represents a 1-Kbyte memory range.
3. Enable base controller configuration:
    a) PCI "Bus Master IDE Base I/O Address" register (ICH Function 1 PCI Config. Offset 20–23h) has been assigned to a 16-bit Base I/O Address.
    b) PCI Command Register (ICH Function 1 PCI Config. Offset 04h): bit 0 is 1, bit 2 is 1.
    c) "IDE Decode Enable" bit is 1 for each enabled controller
    d) Primary Controller: ICH Function 1 PCI Cfg. Offset 40h, bit 15 is 1.
    e) Secondary Controller: ICH Function 1 PCI Cfg. Offset 42h, bit 15 is 1.
4. For each enabled controller, determine the presence of drives and their capabilities:
    a) ATA Devices: IDENTIFY_DRIVE Command (0xEC)
    b) ATAPI Devices: IDENTIFY_DEVICE Command (0xA1)
5. For each device detected, identify the drive's mode capabilities:

a) Determine Fastest Ultra DMA mode (if Ultra DMA is supported) by the drive.

b) Determine Fastest DMA Mode (if DMA is supported) by the drive.

c) Determine fastest PIO mode supported by the drive.

d) This step (d) is to be completed for ICH, ICH2, ICH3, ICH4, and ICH5 (ICH0 may bypass this step).

For BIOS Initialization:

If the device is capable of Ultra DMA modes 3, 4 or 5, the BIOS must determine the cable type for each device. The results shall be put into the IDE I/O Configuration register (ICH IDE PCI Config. Offset 54h, bits 4–7). The presence of an 80-conductor cable shall be indicated in this register by the corresponding device's bit set to a 1, whereas the presence of a 40-conductor cable shall be indicated in this register by the corresponding device's bit cleared to a 0.

For Operating System Driver Initialization:

If the device is capable of Ultra DMA modes 3, 4 or 5, check the IDE I/O Configuration register (ICH IDE PCI Config. Offset 54h, bits 4-7) for the presence of an 80-conductor cable. Note that BIOS must detect the presence of an 80-conductor ATA cable and set the appropriate bits in PCI Config. Offset 54h. Presence of the 80-conductor cable shall allow enabling of Ultra DMA modes 3, 4 and 5, whereas absence of the 80-conductor cable (presence of a 40-cond. cable) shall limit operation of the device to Ultra DMA modes 0, 1 or 2.

Tips:

- Since the "best DMA mode" and "best PIO modes" share the same timing bits, ensure that a comparable mode is selected.

6. Depending on the detected drive capabilities program, the drives for the selected modes using the ATA SET_FEATURES command with the appropriate set transfer mode sub-commands can be set as the following:

    a) Set Features to set current PIO timing mode.

    b) Set Features to set current DMA timing mode.

        i. If Ultra DMA protocol is supported by the device, Set Features to set current Ultra timing mode.

        -ELSE-

        ii. If multi-word DMA protocol is supported by the device, Set Features to set current multi-word DMA timing mode.

        -ELSE-

        iii. If single-word DMA protocol is supported by the device, Set Features to set current single-word DMA timing mode.

Tips:

- In the case that the Set Features command to set the Ultra DMA timing mode fails, the drive's DMA timing mode should be programmed according to its multi-word DMA timing mode.
- In the case that Ultra DMA is not supported on the drive **and** the multi-word /single-word DMA timing mode **cannot** be set on a drive, the driver should be accessed in PIO mode only.
- A Set Features command must be successfully executed to indicate in which mode the drive should be. If a Set Features command completely fails, then the timing mode shall not be enabled or operated.

7. Program the ICH ATA Controller for the selected drive timings:

    a) IDE Timing Register (PCI Config. Offsets 40-41h, 42-43h, 44h) is programmed to reflect the optimum PIO and/or multi-word DMA timing modes for the drives programmed in the previous steps.

    b) Program Ultra DMA Timing Registers (PCI Config. Offsets 48h, 4A-4Bh) if Ultra DMA was enabled for any of the drives in the previous steps. Note that 4A-4Bh shall take into account the settings for Ultra DMA modes 0-5.

    c) Program Bus Master IDE Status Bits to indicate drive DMA capabilities for the drives on the system.

        i. If a given drive is configured for an Ultra DMA mode, the drive's corresponding DMA capable bit should be 1.

        ii. If a given drive is configured for a multi-word DMA or single-word DMA mode, the drive's corresponding DMA capable bit should be 1.

        iii. If a given drive, is not configured for an Ultra DMA or multi-word DMA mode or single-word DMA mode (the drive is PIO only), the drive's corresponding DMA capable bit should be "0."

    d) Program the ATA/100 and ATA/66 Base Clock control bits based on the selected UDMA mode

        i. If UDMA mode 5 is selected, program the ATA/100 Base Clock control bits (PCI Config. Offset 54h, bits 12-15, also called FAST_SCB0/1 and FAST_PCB0/1)

        ii. If UDMA mode 3 or 4 is selected, program the ATA/66 Base Clock control bits (PCI Config. Offset 54h, bits 0-3, also called SCB0/1 and PCB0/1)

        iii. If UDMA mode 0, 1 or 2 is selected, ensure that both the ATA/100 and ATA/66 Base Clock control bits are clear.

Program the WR_PingPong_EN bit (PCI Config. Offset 54h, bit 10) to a 1.

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4 Intel® ICH ATA Controller Configuration Registers

4.1 Register Overview

This section will list out the entire supported PCI configuration space registers and "Bus Master I/O" registers, with details of individual bit definitions and their respective programming being left to the *Register Programming Specifics* Section (4.2) that follows.

4.1.1 Intel® ICH ATA Controller PCI Configuration Registers

Table 7. PCI Configuration Registers

Offset	Register Name/Function	Register Type
00-01	Vendor ID	RO
02-03	Device ID	RO
04-05	Command Register	R/W
06-07	Device Status	R/W
08	Revision ID	RO
09	Programming Interface (Read-Only for ICH0, ICH, and ICH2, but Read-Write for ICH5, ICH4 and ICH3)	RO or RW
0A	Sub Class Code	RO
0B	Base Class Code	RO
0C	Reserved (Cache Line Size)	RO
0D	Master Latency Timer	R/W
0E	Header Type	RO
0F	Reserved	RO
10-13	Primary Command Task File Base Address Register (new for ICH5, ICH4 and ICH3)	R/W
14-17	Primary Control Task File Base Address Register (new for ICH5, ICH4 and ICH3)	R/W
18-1B	Secondary Command Task File Base Address Register (new for ICH5, ICH4 and ICH3)	R/W
1C-1F	Secondary Control Task File Base Address Register (new for ICH5, ICH4 and ICH3)	R/W
20–23	Bus Master IDE Base Address Register	R/W

Offset	Register Name/Function	Register Type
24–27	Expansion BAR	R/W
28:2B	Reserved	RO
2C:2D	Subsystem Vendor ID (ICH2, ICH3, ICH4, and ICH5)	R/W-Once
2E:2F	Subsystem ID (ICH2, ICH3, ICH4, and ICH5)	R/W-Once
24–3B	Reserved	RO
3C	Interrupt Line (new for ICH5, ICH4 and ICH3)	R/W
3D	Interrupt Pin (new for ICH5, ICH4 and ICH3)	RO
3F	Reserved	RO
40–41	IDE TIMING (Primary)	R/W
42–43	IDE TIMING (Secondary)	R/W
44	Slave IDE Timing (Primary and Secondary)	R/W
45:47	Reserved	RO
48	Ultra DMA Control Register	R/W
49	Reserved	RO
4A:4B	Ultra DMA Timing Register	R/W
4C-53	Reserved	RO
54:55	IDE I/O Configuration (New for the “ICH family,” changes for ICH2, ICH3, ICH4, and ICH5)	R/W
56–F7	Reserved	RO
F8–FB	Manufacturer's ID	RO
FC-FF	Reserved	RO

4.1.2 Intel® ICH ATA Controller Bus Master IDE I/O Registers

Table 8. Bus Master IDE I/O Registers

Offset from Base Address	Register	Register Access
00h	Bus Master IDE Command register Primary (BMICP)	R/W
01h	Reserved	Reserved
02h	Bus Master IDE Status register Primary (BMISP)	RO
03h	Reserved	Reserved
04h-07h	Bus Master IDE PRD Table Address Primary (BMIPRDP)	R/W
08h	Bus Master IDE Command register Secondary (BMICS)	R/W
09h	Reserved	
0Ah	Bus Master IDE Status register Secondary (BMISS)	RO
0Bh	Reserved	Reserved
0Ch-0Fh	Bus Master IDE PRD Table Address Secondary (DMIPRDS)	R/W

4.2 Register Programming Specifics

This section will describe each of the PCI configuration space registers and "Bus Master I/O" registers and their respective programming.

4.2.1 General Configuration Registers

The following register bit layout maps define the general configuration registers of the ICH ATA controller, which define how to enable the DMA engine and select the BAR address and bus type (memory or IO) used for the "Bus Master IDE I/O" space.

Table 9. PCI Command Register (ICH Function 1 PCI Config. Offset 04-05h)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													**Bus Master Enable**	**Memory Space Enable**	**I/O Space Enable**
Default = 0													0: Disabled **1: Enabled**	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled

Tips:

- For ICH, ICH0, and ICH2, the "Bus Master Enable" and "I/O Space Enable" bits must be set to 1 for proper operation of these controllers.
- Additionally, for ICH5, ICH4 and ICH3 the "Memory Space Enable" bits must be set to 1 for proper operation of this controller.
- The appropriate BARs must be programmed before setting either the "I/O Space Enable" or "Memory Space Enable" bits.

Table 10. PCI Programming Interface Register (ICH Function 1 PCI Config. Offset 09h)

7	6	5	4	3	2	1	0
Bus Master Support Indicator	**Reserved**			**Secondary Capabilities**	**Secondary Mode Select**	**Primary Capabilities**	**Primary Mode Select**
1: Indicates that bus master operation is supported	**0: Compatibility Enabled** 1: Native PCI Enabled			0: Compatibility Only Supported 1: Native and Compatibility Supported	**0: Compatibility Enabled** 1: Native PCI Enabled	0: Compatibility Only Supported 1: Native and Compatibility Supported	**0: Compatibility Enabled** 1: Native PCI Enabled

Tips:

- The Primary/Secondary Mode Select bits allow PCI Enable only for ICH5, ICH4 and ICH3.
- The Primary/Secondary Capabilities indicators are "Read-Only" bits, where a 1 indication is only available with ICH5, ICH4 and ICH3.

Table 11. PCI Primary Command Task File Base I/O Address Register (ICH Fn 1 PCI Config. Offset 10-13h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Bus Master IDE Base I/O Address, bits 31:16															
0000h: (RO) The bits that correspond to I/O AD[31:16] are hardwired to 0000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Bus Master IDE Base I/O Address, bits 15:4												**Reserved**			**Resource Type Indicator**
0000h: These bits provide the base address for the Bus Master interface registers and correspond to I/O AD[15:4]												**000h**			**1 (RO): I/O Address**

Tips:

- When either Compatibility or Native PCI mode is programmed, the "Resource Type Indicator" will report a 1. This indicates the BAR must be filled out, regardless of which mode is programmed by BIOS, since it is not known into what mode an OS may put the controller.
- Allocation of the BAR requires a sequence defined in the *PCI Local Bus Specification, Revision 2.3*. This register will indicate the need for eight consecutive I/O locations.
- ATA controller identification of I/O accesses will be valid after writing a valid 16-bit I/O address to this register when Native PCI mode is enabled and when the PCI "Command" has the "I/O Space Enable" bit set.

Table 12. PCI Primary Control Task File Base I/O Address Register (ICH Fn 1 PCI Config. Offset 14-17h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Bus Master IDE Base I/O Address, bits 31:16															
0000h: (RO) The bits that correspond to I/O AD[31:16] are hardwired to 0000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Bus Master IDE Base I/O Address, bits 15:4												**Reserved**			**Resource Type Indicator**
0000h: These bits provide the base address for the Bus Master interface registers and correspond to I/O AD[15:4]												**000h**			**1 (RO): I/O Address**

Tips:

- When either Compatibility or Native PCI mode is programmed, the "Resource Type Indicator" will report a 1. This indicates the BAR must be filled out, regardless of which mode is programmed by BIOS, since it is not known into what mode an operating system may put the controller.
- Allocation of the BAR requires a sequence defined in the *PCI Local Bus Specification, Revision 2.3*. This register will indicate the need for four, consecutive I/O locations.
- ATA controller identification of I/O accesses will be valid after writing a valid 16-bit I/O address to this register when Native PCI mode is enabled and when the PCI "Command" has the "I/O Space Enable" bit set.

Table 13. PCI Secondary Command Task File Base I/O Address Register (ICH Fn 1 PCI Config. Offset 18-1Bh)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Bus Master IDE Base I/O Address, bits 31:16															
0000h: (RO) The bits that correspond to I/O AD[31:16] are hardwired to 0000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Bus Master IDE Base I/O Address, bits 15:4												**Reserved**			**Resource Type Indicator**
0000h: These bits provide the base address for the Bus Master interface registers and correspond to I/O AD[15:4]												**000h**			**1 (RO): I/O Address**

Tips:

- When either Compatibility or Native PCI mode is programmed, the "Resource Type Indicator" will report a 1. This indicates the BAR must be filled out, regardless of which mode is programmed by BIOS, since it is not known into what mode an operating system may put the controller.
- Allocation of the BAR requires a sequence defined in the *PCI Local Bus Specification, Revision 2.3*. This register will indicate the need for eight, consecutive I/O locations.
- ATA controller identification of I/O accesses will be valid after writing a valid 16-bit I/O address to this register when Native PCI mode is enabled and when the PCI "Command" has the "I/O Space Enable" bit set.

Table 14. PCI Secondary Control Task File Base I/O Address Register (ICH Fn 1 PCI Config. Offset 1C-1Fh)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Bus Master IDE Base I/O Address, bits 31:16															
0000h: (RO) The bits that correspond to I/O AD[31:16] are hardwired to 0000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Bus Master IDE Base I/O Address, bits 15:4												**Reserved**			**Resource Type Indicator**
0000h: These bits provide the base address for the Bus Master interface registers and correspond to I/O AD[15:4]												**000h**			**1 (RO): I/O Address**

Tips:

- When either Compatibility or Native PCI mode is programmed, the "Resource Type Indicator" will report a 1. This indicates the BAR must be filled out, regardless of which mode is programmed by BIOS, since it is not known into what mode an OS may put the controller.
- Allocation of the BAR requires a sequence defined in the *PCI Local Bus Specification, Revision 2.3*. This register will indicate the need for 4 consecutive I/O locations.
- ATA controller identification of I/O accesses will be valid after writing a valid 16-bit I/O address to this register when Native PCI mode is enabled and when the PCI "Command" has the "I/O Space Enable" bit set.

Table 15. PCI Bus Master IDE Base I/O Address Register (ICH Fn 1 PCI Config. Offset 20–23h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Bus Master IDE Base I/O Address, bits 31:16															
0000h: (RO) The bits that correspond to I/O AD[31:16] are hardwired to 0000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Bus Master IDE Base I/O Address, bits 15:4												**Reserved**			**Resource Type Indicator**
0000h: These bits provide the base address for the Bus Master interface registers and correspond to I/O AD[15:4]												**000h**			**1 (RO): I/O Address**

Tips:

- When either Compatibility or Native PCI mode is programmed, the "Resource Type Indicator" will report a 1. This BAR must be filled out, regardless of which mode is programmed by BIOS, since DMA is used in either Compatibility or Native PCI modes.
- Allocation of the BAR requires a sequence defined in the *PCI Local Bus Specification, Revision 2.3*. This register will indicate the need for 16 consecutive I/O locations.
- ATA controller identification of I/O accesses will be valid after writing a valid 16-bit I/O address to this register when Native PCI mode is enabled and when the PCI "Command" has the "I/O Space Enable" bit set.

Table 16. PCI Expansion Base Memory Address Register (ICH Fn 1 PCI Config. Offset 24–27h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Bus Master IDE Base I/O Address, bits 31:16															
0000h: These bits provide the base address for the Expansion interface registers and correspond to Memory AD[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Expansion Base Memory Address, bits 15:4												Pre-Fetch	**Type**		**Resource Type Indicator**
0000h: These bits provide the base address for the Expansion interface registers and correspond to Memory AD[15:4]												0h (RO): No Pre-fetch	**00h (RO): 32-bit mapping**		**0 (RO): Memory Address**

Tips:

- When either Compatibility or Native PCI mode is programmed, the "Resource Type Indicator" will report a 0. This bit is read-only.
- When either Compatibility or Native PCI mode is programmed, the "Type" bit will report a "00", indicating that the BAR can be mapped anywhere in 32-bit address space. This bit is read-only.
- When either Compatibility or Native PCI mode is programmed, the "Pre-Fetchable" bit will report a 0, indicating that the range is not pre-fetchable. This bit is read-only.
- Allocation of the bar requires a sequence defined in the *PCI Local Bus Specification, Revision 2.3*. This register will indicate the need for 1-Kbyte consecutive memory locations.

- ATA controller identification of memory accesses will be valid after writing a valid 32-bit memory address to this register and when the PCI "Command" has the "Memory Space Enable" bit set.

Table 17. IDE Subsystem Vendor ID Register (ICH Fn 1 PCI Config. Offset 2C–2Dh)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Subsystem Vendor ID, Write-Once by BIOS at Boot															
Default = 0															

Tips:

- This is a "Read and Write-Once" register.
- BIOS sets the value in this register to identify the Subsystem Vendor ID, which enable the OS to distinguish subsystems from each other.
- This register is only available on ICH2, ICH3, ICH4, and ICH5.

Table 18. IDE Subsystem ID Register (ICH Fn 1 PCI Config. Offset 2E–2Fh)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Subsystem ID, Write-Once by BIOS at Boot															
Default = 0															

Tips:

- This is a "Read and Write-Once" register.
- BIOS sets the value in this register (in conjunction with the Subsystem Vendor ID register) to identify the Subsystem ID, which enable the OS to distinguish subsystems from each other.
- The valued written in this register will also be readable to the corresponding SID registers for the USB #1, USB #2 and SMBus functions.
- This register is only available on ICH2, ICH3, ICH4, and ICH5.

Table 19. Interrupt Line Register (ICH Fn 1 PCI Config. Offset 3Ch)

7	6	5	4	3	2	1	0
Interrupt Line, Write by BIOS at Boot							
Default = 0							

Tips:

- This is a "Read and Write-Once" register.
- BIOS sets the value in this register to communicate to software the Native PCI Interrupt line that the interrupt pin is connected to when the controller is programmed for Native PCI operation.
- This register is only available on ICH3, ICH4, and ICH5.

Table 20. Interrupt Line Register (ICH Fn 1 PCI Config. Offset 3Dh)

7	6	5	4	3	2	1	0
Interrupt Line, Write by BIOS or OS enumerator at Boot							
Default = 1 (RO)							

Tips:

- This is a "Read-Only" register, indicating to software that the device will drive PIRQ[A].
- This is only used when native PCI mode is enabled.
- The routine to the internal interrupt controller doesn't necessarily relate to the value in this register. The IDE interrupt is in fact routed to PIRQ[C]# (IRQ18 in APIC mode).
- This register is only available on ICH3, ICH4 and ICH5.

4.2.2 PIO and DMA Mode Timing and Control Registers

The following register bit layout maps define the specific ATA controller device timing and mode configuration registers. These registers control PIO timings as well as single- and multi-word DMA timings for the master device on the primary and secondary controllers.

Table 21. IDETIM1 and IDETIM2

15	14	13	12	11	10	9	8
IDE Decode Enable	**Slave IDE Timing Register Enable (SITRE)**	**IORDY Sample Point (ISP)**		**Reserved**		**Recovery Time**	
0: Disabled 1: Enabled	**0: Disabled** 1: Enabled	00: 5 clocks 01: 4 clocks 10: 3 clocks 11: 2 clocks		00h		00: 4 clocks 01: 3 clocks 10: 2 clocks 11: 1 clock	

7	6	5	4	3	2	1	0
DMA Timing Enable Only Select 1 (DTE1)	**Pre-fetch and Posting Enable Select 1 (PPE1)**	**IORDY Sample Point Enable Select 1 (IE1)**	**Fast Timing Bank Drive Select 1 (TIME1)**	**DMA Timing Enable Only Select 0 (DTE0)**	**Pre-fetch and Posting Enable Select 0 (PPE0)**	**IORDY Sample Point Enable Select 0 (IE0)**	**Fast Timing Bank Drive Select 0 (TIME0)**
0: Disabled 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled

NOTES:
IDETIM1 = IDE Timing Register 1 (Primary: ICH Fn 1 PCI Config. Offset 40-41h)
IDETIM2 = IDE Timing Register 2 (Secondary: ICH Fn 1 PCI Config. Offset 42-43h)

Tips:

- The ***DMA Timing Enable Only Select*** bit is:
  Enabled (1) if and only if the device's PIO capability is much slower than its DMA capability.

- The ***Pre-fetch and Posting Enable Select*** bit is:
  Enabled (1) if and only if the device is a fixed disk.
- The ***IORDY Sample Point Enable Select*** bit is:
  Enabled (1) depending on the current mode and capabilities of the drive, according to the device's capabilities for PIO Mode 2, and (2) always Enabled for IORDY Modes (PIO3 and greater). The value of this bit has no effect when applicable Fast Timing Bank Select is disabled.
- The ***Fast Timing Bank Drive Select*** bit is:
  Enabled (1) if the drive mode is Mode 2 or greater (>Compatible).

Table 22. SITR – Slave IDE Timing Register (ICH Fn 1 PCI Config. Offset 44h)

7	6	5	4	3	2	1	0
Secondary Slave IORDY Sample Point		**Secondary Slave Recovery Time**		**Primary Slave IORDY Sample Point**		**Primary Slave Recovery Time**	
00: 5 clocks 01: 4 clocks 10: 3 clocks 11: 2 clocks		00: 4 clocks 01: 3 clocks 10: 2 clocks 11: 1 clock		00: 5 clocks 01: 4 clocks 10: 3 clocks 11: 2 clocks		00: 4 clocks 01: 3 clocks 10: 2 clocks 11: 1 clock	

Tips:

- The ***IDE Decode Enable*** field determines whether or not the cable is enabled:
  Primary Controller: ICH Function 1 PCI Config. Offset 40h, bit 15
  Secondary Controller: ICH Function 1 PCI Config. Offset 42h, bit 15
- The ***IORDY Sample Point and Recovery Time*** fields specify the current IDE timing cycle times.
- The ***Slave IDE Timing Register*** bit is:
  Disabled by default. This bit needs to be enabled to take advantage of the ICH timings when a slave drive is attached to this cable. When this field is disabled, the ICH Slave IDE Timing Register is disabled.

Table 23. BMIC1 and BMIC2

7	6	5	4	3	2	1	0
Reserved				**Bus Master Read/Write Control (RWCON)**	**Reserved**		**Start/Stop Bus Master (SSBM)**
0000h				**0: Read** 1: Write Sets direction for transfers.	00h		**0: Stop** 1: Start Starts & Stops DMA transfer engine.

NOTES:
BMIC1 = Bus Master IDE Control Register 1 (Primary: Bus Master IDE Base I/O Address + Offset 0h)
BMIC2 = Bus Master IDE Control Register 2 (Secondary: Bus Master IDE Base I/O Address + Offset 8h)

Tips:

- The ***Bus Master Read/Write Control*** bit shall set the transfer direction for DMA transfers. This bit must NOT be changed when the bus master function is active. While an Ultra DMA transfer is in progress, this bit will be READ ONLY. The bit will return to read/write once the synchronous DMA transfer has been completed or halted.
- The ***Start/Stop Bus Master*** bit shall be the control method to start or stop the DMA transfer engine. When this bit is set to 1, bus master operation starts. The controller transfers data between the IDE device and memory only while this bit is set. Master operation can be stopped by writing a 0 to this bit. This results in all state information being lost (i.e., master mode operation cannot be stopped and then resumed).

Table 24. BMIS1 and BMIS2

7	6	5	4	3	2	1	0
Reserved	**Drive 1 DMA Capable (DMACAP1)**	**Drive 0 DMA Capable (DMACAP0)**	**Reserved**		**IDE Interrupt Status (IDEINTS)**	**IDE DMA Error**	**Bus Master IDE Active (BMIDEA)**
0h	**0: Drive is PIO only.** 1: Drive is capable and configured for DMA transfers.	**0: Drive is PIO only.** 1: Drive is capable and configured for DMA transfers.	00h		**0: R/W/C** Software writes 1 to clear.	**0: R/W/C** Software writes 1 to clear.	**0: RO**

NOTES:
BMIS1 = Bus Master IDE Status Register 1 (Primary: Bus Master IDE Base I/O Address + Offset 02h)
BMIS2 = Bus Master IDE Status Register 2 (Secondary: Bus Master IDE Base I/O Address + Offset 0Ah)

Tips:

- The ***Drive 0 DMA Capable*** bit shall be:
  Set to 1 when the Drive 0 (Master) has been identified and configured for DMA transfers (Ultra DMA, multi-word DMA or single-word DMA).
  Set to 0 if Drive 0 is PIO only and/or not configured for DMA operation.
- The ***Drive 1 DMA Capable*** bit shall be:
  Set to 1 when the Drive 1 (Slave) has been identified and configured for DMA transfers.
  Set to 0 if Drive 1 is PIO only and/or not configured for DMA operation.

It is the responsibility of initialization software to ensure that these DMA capable bits are set so that a PCI Bus Master IDE device driver can determine which drives have been configured for DMA operation. More details on the BMIC and BMIS registers are detailed in the “Bus Master IDE Command and Status Register” section of this document.

4.2.3 Ultra DMA Configuration of Timing and Control Registers

The following register bit layout maps define the specific ATA controller device timing and mode configuration registers for Ultra DMA operation on all devices. These registers are programmed in systems that contain devices that implement the Ultra DMA protocol. These registers allow Ultra DMA to be used when DMA operation is initiated by the device driver.

Table 25. UDMAC - Ultra DMA Control Register (ICH Function 1 PCI Config. Offset 48h)

7	6	5	4	3	2	1	0
Reserved				Secondary Drive 1 Ultra DMA Mode Enable (SSDE1)	Secondary Drive 0 Ultra DMA Mode Enable (SSDE0)	Primary Drive 1 Ultra DMA Mode Enable (PSDE1)	Primary Drive 0 Ultra DMA Mode Enable (PSDE0)
0000h				**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled	**0: Disabled** 1: Enabled

Tips:

- ***The Ultra DMA Enable*** bit specifies the current Ultra DMA enabled status:
  Disabled by default: This field needs to be enabled in order to take advantage of the ICH Ultra DMA timings. When this field is disabled, **the ICH Ultra DMA Timing Register is disabled**.

Table 26. UDMATIM - Ultra DMA Timing Register (ICH Function 1 PCI Config. Offsets 4A-4Bh)

15	14	13	12	11	10	9	8
Reserved		**Secondary Drive 1 Ultra DMA Cycle Time (SCT1)**		**Reserved**		**Secondary Drive 0 Ultra DMA Cycle Time (SCT0)**	
00h		**SCB1 = 0 (and) FAST_SCB1 = 0 (33MHz base clock)** 00: CT=4 clks, RP=6 clks 01: CT=3 clks, RP=5 clks 10: CT=2 clks, RP=4 clks 11: Reserved **SCB1 = 1 (and) FAST_SCB1 = 0 (66MHz base clock)** 00: Reserved 01: CT=3 clks, RP=8 clks 10: CT=2 clks, RP=8 clks 11: Reserved **SCB1 = X (and) FAST_SCB1 = 1 (100MHz base clock)** 00: Reserved 01: CT=3 clks, RP=16 clks 10: Reserved 11: Reserved		00h		**SCB0 = 0 (and) FAST_SCB0 = 0 (33MHz base clock)** 00: CT=4 clks, RP=6 clks 01: CT=3 clks, RP=5 clks 10: CT=2 clks, RP=4 clks 11: Reserved **SCB0 = 1 (and) FAST_SCB0 = 0 (66MHz base clock)** 00: Reserved 01: CT=3 clks, RP=8 clks 10: CT=2 clks, RP=8 clks 11: Reserved **SCB0 = X (and) FAST_SCB0 = 1 (100MHz base clock)** 00: Reserved 01: CT=3 clks, RP=16 clks 10: Reserved 11: Reserved	

7	6	5	4	3	2	1	0
Reserved		**Primary Drive 1 Ultra DMA Cycle Time (PCT1)**		**Reserved**		**Primary Drive 0 Ultra DMA Cycle Time (PCT0)**	
00h		**PCB1 = 0 (and) FAST_PCB1 = 0 (33MHz base clock)** 00: CT=4 clks, RP=6 clks 01: CT=3 clks, RP=5 clks 10: CT=2 clks, RP=4 clks 11: Reserved **PCB1 = 1 (and) FAST_PCB1 = 0 (66MHz base clock)** 00: Reserved 01: CT=3 clks, RP=8 clks 10: CT=2 clks, RP=8 clks 11: Reserved **PCB1 = X (and) FAST_PCB1 = 1 (100 MHz base clock)** 00: Reserved 01: CT=3 clks, RP=16 clks 10: Reserved 11: Reserved		00h		**PCB0 = 0 (and) FAST_PCB0 = 0 (33MHz base clock)** 00: CT=4 clks, RP=6 clks 01: CT=3 clks, RP=5 clks 10: CT=2 clks, RP=4 clks 11: Reserved **PCB0 = 1 (and) FAST_PCB0 = 0 (66MHz base clock)** 00: Reserved 01: CT=3 clks, RP=8 clks 10: CT=2 clks, RP=8 clks 11: Reserved **PCB0 = X (and) FAST_PCB0 = 1 (100 MHz base clock)** 00: Reserved 01: CT=3 clks, RP=16 clks 10: Reserved 11: Reserved	

Tips:

- The ***Ultra DMA Cycle Time Field*** specifies the current Ultra DMA timing mode.

Note: This field only applies if the corresponding Ultra DMA Enable field is set.

Table 27. IDE I/O Configuration - (ICH PCI Config. Offset 54-55h)

15	14	13	12	11	10	9	8
FAST Secondary Drive 1 Base Clock (FAST_SCB1)	**FAST Secondary Drive 0 Base Clock (FAST_SCB0)**	**FAST Primary Drive 1 Base Clock (FAST_PCB1)**	**FAST Primary Drive 0 Base Clock (FAST_PCB0)**	**Reserved**	**WR_Ping-Pong_EN**	**Reserved**	
0: 33MHz or 66MHz Clock 1: 100 MHz Clock	**0: 33MHz or 66MHz Clock** 1: 100 MHz Clock	**0: 33MHz or 66MHz Clock** 1: 100 MHz Clock	**0: 33MHz or 66MHz Clock** 1: 100 MHz Clock	0h	**0: Disabled** 1: Enabled	00h	

7	6	5	4	3	2	1	0
Secondary Drive 1 Cable Reporting (SCR1)	**Secondary Drive 0 Cable Reporting (SCR0)**	**Primary Drive 1 Cable Reporting (PCR1)**	**Primary Drive 0 Cable Reporting (PCR0)**	**Secondary Drive 1 Base Clock (SCB1)**	**Secondary Drive 0 Base Clock (SCB0)**	**Primary Drive 1 Base Clock (PCB1)**	**Primary Drive 0 Base Clock (PCB0)**
0: 40-conductor Cable Present 1: 80-conductor Cable Present	**0: 40-conductor Cable Present** 1: 80-conductor Cable Present	**0: 40-conductor Cable Present** 1: 80-conductor Cable Present	**0: 40-conductor Cable Present** 1: 80-conductor Cable Present	**0: 33 MHz Clock** 1: 66 MHz Clock	**0: 33 MHz Clock** 1: 66 MHz Clock	**0: 33 MHz Clock** 1: 66 MHz Clock	**0: 33 MHz Clock** 1: 66 MHz Clock

Tips:

- The ***WR_PingPong_EN*** bit should always be set to a 1. This is to enable a performance enhancement feature for PIO transfers. Clearing this bit to 0 will result in performance and functionality similar to PIO on the PIIX family of ATA Controllers.
- ***Base Clock*** bit(s) specify if the UDMATIM register indicates Ultra ATA/100, Ultra ATA/66 or Ultra ATA/33 timings.
- ***Cable Reporting*** bit(s) specifies the presence of an 80-conductor cable (set to 1) or 40-conductor cable (cleared to 0). This information shall be filled in by system BIOS, and interpreted by both BIOS and system OS drivers. As per the Ultra ATA/100 and Ultra ATA/66 specification(s), no drive shall be programmed to Ultra DMA modes 3, 4 or 5 unless an 80-conductor cable is present. In the presence of a 40-conductor cable, all devices shall be limited to Ultra DMA mode 2 or less.

5 Determining a Drive's Transfer Rate Capabilities

5.1 Overview

The following section provides the information that allows a drive's capabilities to be determined.

The ATA IDENTIFY_DRIVE (0xEC) and ATAPI IDENTIFY_DEVICE (0x1A) can be used to determine the capability. Each of these commands return a 256-word buffer with fields that can allow the drive's capabilities to be determined.

Refer to the ATA Specification for more information regarding the IDENTIFY_DEVICE command.

Table 28. Identify Device Information Used for Determining Drive Capabilities

Capability	Word Offset	Bits	Field
Device Type			***Fields that Indicate Device Type***
Device Type	0	15	General Configuration: 0: ATA Device 1: ATAPI Device
Ultra DMA			***Fields that Indicate Ultra DMA Drive Capabilities***
Ultra DMA	53	2	Field Validity 0: the fields reported in word 88 are not valid 1: the fields reported in word 88 are valid

Capability	Word Offset	Bits	Field
Ultra DMA	88	13:8	Ultra DMA Modes Active* bit 13: 1: Ultra DMA Mode 5 is active 0: Ultra DMA Mode 5 is not active bit 12: 1: Ultra DMA Mode 4 is active 0: Ultra DMA Mode 4 is not active bit 11: 1: Ultra DMA Mode 3 is active 0: Ultra DMA Mode 3 is not active bit 10: 1: Ultra DMA Mode 2 is active 0: Ultra DMA Mode 2 is not active bit 9: 1: Ultra DMA Mode 1 is active 0: Ultra DMA Mode 1 is not active bit 8: 1: Ultra DMA Mode 0 is active 0: Ultra DMA Mode 0 is not active
Ultra DMA	88	5:0	Ultra DMA Modes Supported* bit 5: 1: Ultra DMA Mode 5 is supported 0: Ultra DMA Mode 5 is not supported bit 4: 1: Ultra DMA Mode 4 is supported 0: Ultra DMA Mode 4 is not supported bit 3: 1: Ultra DMA Mode 3 is supported 0: Ultra DMA Mode 3 is not supported bit 2: 1: Ultra DMA Mode 2 is supported 0: Ultra DMA Mode 2 is not supported bit 1: 1: Ultra DMA Mode 1 is supported 0: Ultra DMA Mode 1 is not supported bit 0: 1: Ultra DMA Mode 0 is supported 0: Ultra DMA Mode 0 is not supported
DMA			***Fields that Indicate Multi Word DMA/Single-Word DMA Drive Capabilities***
PIO, DMA	53	1	Field Validity 0: the fields reported in words 64-70 are not valid 1: the fields reported in word 64-70 are valid

Capability	Word Offset	Bits	Field
DMA	62	10:8	Single-Word DMA Modes Active bit 10: 1: Single-Word DMA Mode 2 is active 0: Single-Word DMA Mode 2 is not active bit 9: 1: Single-Word DMA Mode 1 is active 0: Single-Word DMA Mode 1 is not active bit 8: 1: Single-Word DMA Mode 0 is active 0: Single-Word DMA Mode 0 is not active
DMA	62	2:0	Single-Word DMA Modes Supported bit 2: 1: Single-Word DMA Mode 2 is supported 0: Single-Word DMA Mode 2 is not supported bit 1: 1: Single-Word DMA Mode 1 is supported 0: Single-Word DMA Mode 1 is not supported bit 0: 1: Single-Word DMA Mode 0 is supported 0: Single-Word DMA Mode 0 is not supported
DMA	63	10:8	Multi-Word DMA Modes Active bit 10: 1: Multi-Word DMA Mode 2 is active 0: Multi-Word DMA Mode 2 is not active bit 9: 1: Multi-Word DMA Mode 1 is active 0: Multi-Word DMA Mode 1 is not active bit 8: 1: Multi Word DMA Mode 0 is active 0: Multi-Word DMA Mode 0 is not active
DMA	63	2:0	Multi-Word DMA Modes Supported bit 2: 1: Multi-Word DMA Mode 2 is supported 0: Multi-Word DMA Mode 2 is not supported bit 1: 1: Multi-Word DMA Mode 1 is supported 0: Multi-Word DMA Mode 1 is not supported bit 0: 1: Multi-Word DMA Mode 0 is supported 0: Multi-Word DMA Mode 0 is not supported
DMA	65	15:0	Minimum Multi-Word DMA Transfer Cycle Time Per Word
DMA	66	15:0	Manufacturer's recommended Multi-Word DMA Transfer Cycle Time
PIO			***Fields that Indicate PIO Drive Capabilities***
PIO	51	15:8	PIO Data Transfer Cycle Timing Mode Supported 00h: PIO0 01h: PIO1 02h: PIO2

Capability	Word Offset	Bits	Field
PIO, DMA	53	1	Field Validity 0: the fields reported in words 64-70 are not valid 1: the fields reported in word 64-70 are valid
PIO	64	7:0	Advanced Flow Control PIO Transfer Modes Supported bit 0: PIO3 (w/IORDY Flow Control) bit 1: PIO4 (w/IORDY Flow Control)
PIO	67	15:0	Minimum PIO Transfer Cycle Time without Flow Control
PIO	68	15:0	Minimum PIO Transfer Cycle Time with IORDY Flow Control

For ICH ATA Timing Configuration, each of the following things must be determined:

- Drive Type: ATAPI or ATA (non-ATAPI)
- Best DMA Capability, which includes:
    - Best Ultra DMA Capability, **or**
    - Best Multi-Word DMA Capability (if Ultra DMA not supported), **or**
    - Best Single-Word DMA Capability (if neither Ultra DMA nor Multi-Word DMA supported)
- Best PIO Capability

5.2 Determining a Drive's Best Ultra DMA Capability

The drive's Ultra DMA mode capability and current configuration are specified in the IDENTIFY_DRIVE buffer, word offset 88. Software must first check to see that the word offset 88 is valid before determining the Ultra DMA drive capability.

Table 29. Identify Device Information Used for Determining Ultra DMA Drive Capabilities

Capability	Word Offset	Bits	Field
Ultra DMA	53	2	Field Validity 0: the fields reported in word 88 are not valid 1: the fields reported in word 88 are valid
Ultra DMA	88	13:8	Ultra DMA Modes Active(1) bit 13: 1: Ultra DMA Mode 5 is active 0: Ultra DMA Mode 5 is not active bit 12: 1: Ultra DMA Mode 4 is active 0: Ultra DMA Mode 4 is not active bit 11: 1: Ultra DMA Mode 3 is active 0: Ultra DMA Mode 3 is not active bit 10: 1: Ultra DMA Mode 2 is active 0: Ultra DMA Mode 2 is not active bit 9: 1: Ultra DMA Mode 1 is active 0: Ultra DMA Mode 1 is not active bit 8: 1: Ultra DMA Mode 0 is active 0: Ultra DMA Mode 0 is not active
Ultra DMA	88	5:0	Ultra DMA Modes Supported(1) bit 5: 1: Ultra DMA Mode 5 is supported 0: Ultra DMA Mode 5 is not supported bit 4: 1: Ultra DMA Mode 4 is supported 0: Ultra DMA Mode 4 is not supported bit 3: 1: Ultra DMA Mode 3 is supported 0: Ultra DMA Mode 3 is not supported bit 2: 1: Ultra DMA Mode 2 is supported 0: Ultra DMA Mode 2 is not supported bit 1: 1: Ultra DMA Mode 1 is supported 0: Ultra DMA Mode 1 is not supported bit 0: 1: Ultra DMA Mode 0 is supported 0: Ultra DMA Mode 0 is not supported

NOTES:
The following Ultra DMA drive capabilities are supported by the ICH, from fastest to slowest:
– Ultra DMA Mode 5 (ICH2, ICH3, ICH4, and ICH5)
– Ultra DMA Mode 4 (ICH, ICH2, ICH3, ICH4, and ICH5)
– Ultra DMA Mode 3 (ICH, ICH2, ICH3, ICH4, and ICH5)
– Ultra DMA Mode 2
– Ultra DMA Mode 1
– Ultra DMA Mode 0
– Disabled (Drive does not support any of the above Ultra DMA Modes.)

5.3 Determining a Drive's Best Multi- or Single-Word DMA Capability

This section describes how to determine a drive's multi-word DMA and single-word DMA capabilities.

The following DMA drive capabilities are supported by the ICH, from fastest to slowest:

- Multi-Word DMA Mode 2
- Multi-Word DMA Mode 1
- Single-Word DMA Mode 2
- Disabled (Drive does not support any of the above multi- or single-word DMA modes.)

Software at this stage, needs to determine if at least one of the above modes is supported by the drive. Software should initially determine a drive's best multi-word DMA capability initially. If a drive doesn't support multi-word DMA modes 0 or 1, then software should check if single-word DMA mode 2 is supported.

The drive's multi-word DMA mode capability and current configuration are specified in the IDENTIFY_DRIVE buffer, word offsets 63 and 65 Software must first check to see that the word offsets 64–70 are valid before determining the drive's multi-word DMA drive capability. Also check the timing registers of word offsets 65 and 66, limiting the actual mode of operation based on the slowest timing register value and what modes are supported.

The drive's single-word DMA mode capability and current configuration are specified in the IDENTIFY_DRIVE buffer, word offset 62.

Table 30. Identify Device Information Used for Determining Multi-/ Single-Word DMA Drive Capabilities

Capability	Word Offset	Bits	Field
PIO, DMA	53	1	Field Validity 0: the fields reported in words 64-70 are not valid 1: the fields reported in word 64-70 are valid
DMA	62	10:8	Single-Word DMA Modes Active bit 10: 1: Single-Word DMA Mode 2 is active 0: Single-Word DMA Mode 2 is not active bit 9: 1: Single-Word DMA Mode 1 is active 0: Single-Word DMA Mode 1 is not active bit 8: 1: Single-Word DMA Mode 0 is active 0: Single-Word DMA Mode 0 is not active

Capability	Word Offset	Bits	Field
DMA	62	2:0	Single-Word DMA Modes Supported bit 2: 1: Single-Word DMA Mode 2 is supported 0: Single-Word DMA Mode 2 is not supported bit 1: 1: Single-Word DMA Mode 1 is supported 0: Single-Word DMA Mode 1 is not supported bit 0: 1: Single-Word DMA Mode 0 is supported 0: Single-Word DMA Mode 0 is not supported
DMA	63	10:8	Multi-Word DMA Modes Active bit 10: 1: Multi-Word DMA Mode 2 is active 0: Multi-Word DMA Mode 2 is not active bit 9: 1: Multi-Word DMA Mode 1 is active 0: Multi-Word DMA Mode 1 is not active bit 8: 1: Multi-Word DMA Mode 0 is active 0: Multi-Word DMA Mode 0 is not active
DMA	63	2:0	Multi-Word DMA Modes Supported bit 2: 1: Multi-Word DMA Mode 2 is supported 0: Multi-Word DMA Mode 2 is not supported bit 1: 1: Multi-Word DMA Mode 1 is supported 0: Multi-Word DMA Mode 1 is not supported bit 0: 1: Multi-Word DMA Mode 0 is supported 0: Multi-Word DMA Mode 0 is not supported
DMA	65	15:0	Minimum Multi-Word DMA Transfer Cycle Time Per Word

To determine the drive's best DMA capability ensure that the drive reports the capability and is able to transfer at the target cycle time.

Table 31. Drive Multi-Word DMA/Single-Word DMA Capability as a Function of Cycle Time

Drive's Reported DMA Setting	Drives Reported DMA Cycle Time[1]	Drive's Best DMA Mode
Multi-Word DMA Mode 2	t <= 120 ns	Multi-Word DMA Mode 2
Multi-Word DMA Mode 2	120 < t <= 180 ns	Multi-Word DMA Mode 1
Multi-Word DMA Mode 2	180 < t <= 240 ns	Single-Word DMA Mode 2
Multi-Word DMA Mode 2	t > 240 ns	N/A (Disabled)
Multi-Word DMA Mode 1	t <= 180 ns	Multi-Word DMA Mode 1
Multi-Word DMA Mode 1	180 < t <= 240 ns	Single-Word DMA Mode 2
Multi-Word DMA Mode 1	t > 240 ns	N/A (Disabled)
Multi-Word DMA Mode 0	N/A	N/A (Disabled)
Single-Word DMA Mode 2	t <= 240 ns	Single-Word DMA Mode 2
Single-Word DMA Mode 2	t > 114 ns	N/A (Disabled)
Single-Word DMA Mode 1	N/A	N/A (Disabled)
Single-Word DMA Mode 0	N/A	N/A (Disabled)
Drive does not support DMA transfers.	N/A	N/A

NOTES:
1. Timing cycle times are defined by the ATA specification. A device that reports a given DMA mode capability must be capable of supporting the minimum DMA cycle time.

A drive's selected multi-word DMA or single-word DMA speed is the fastest multi-word DMA speed that is supported for the drive. If multi-word DMA is **not** supported for the reported timing cycle time then the drive's best non-Ultra DMA speed is based on its single-word DMA 2 capability.

If N/A is used, the drive is configured for PIO-only. The ICH mode follows the PIO mode only. If a drive does not report a DMA cycle time that is consistent with the Target DMA Cycle Time, a slower speed should be chosen.

The cycle times associated with the various timing modes are defined by the ATA Specification. A drive that reports a given multi-/single-word DMA capability must be capable of supporting the minimum cycle time for that mode.

5.4 Determining a Drive's Best PIO Capability

This section describes how to determine a Drive's PIO Capabilities.

The following PIO drive capabilities are supported by the ICH, from fastest to slowest:

- PIO4 w/IORDY
- PIO3 w/IORDY
- PIO2 w/IORDY
- PIO2 (without IORDY)
- Compatible (Drive does not support any of the above PIO modes.)

Software at this stage needs to determine if at least one of the above modes is supported by the drive. Software should initially determine a drive's best PIO w/IORDY capability (PIO4 w/IORDY or PIO3 w/IORDY) initially. If these PIO w/IORDY modes are not supported, the drive should determine the PIO2 mode support with IORDY or PIO2 mode support without IORDY. Otherwise, Compatible timings should be applied to the drive.

The drive's PIO w/IORDY mode capability is specified in the IDENTIFY_DRIVE buffer, word offsets 64 and 68. Software must first check to see that the word offsets 64–70 are valid before determining the drive's PIO w/IORDY drive capability.

The drive's PIO2 mode capability and current configuration are specified in the IDENTIFY_DRIVE buffer, word offset 51.

Table 32. Identify Device Information Used for Determining PIO Drive Capabilities

Capability	Word Offset	Bits	Field
PIO	51	15:8	PIO Data Transfer Cycle Timing Mode Supported 00h: PIO0 01h: PIO1 02h: PIO2
PIO, DMA	53	1	Field Validity 0: the fields reported in words 64-70 are not valid 1: the fields reported in word 64-70 are valid
PIO	64	7:0	Advanced Flow Control PIO Transfer Modes Supported bit 0: PIO3 (w/IORDY Flow Control) bit 1: PIO4 (w/IORDY Flow Control)
PIO	68	15:0	Minimum PIO Transfer Cycle Time with IORDY Flow Control

To determine the Drive's Best PIO mode, ensure that the drive reports the capability and is able to transfer at the target cycle time:

Table 33. Drive PIO Capability as a Function of Cycle Time

Drive's Reported PIO Mode Setting	Drives Reported PIO Cycle Time[1]	Drive's Best PIO Mode
PIO4	t <= 120 ns	PIO4
PIO4	120 < t <= 180 ns	PIO3
PIO4	180 < t <= 240 ns	PIO2
PIO4	t > 240 ns	PIO0/Compatible
PIO3	t <= 180 ns	PIO3
PIO3	180 < t <= 240 ns	PIO2
PIO3	t > 240 ns	PIO0/Compatible
PIO2	N/A (drive must support t<= 240 ns)	PIO2
PIO1	N/A	PIO0/Compatible
PIO0/Compatible	N/A	PIO0/Compatible

NOTES:
1. Timing cycle times are defined by the ATA specification. A device that reports a given PIO mode capability must be capable of supporting the minimum PIO cycle time.

- The cycle times associated with the various timing modes are defined by the ATA Specification. A drive that reports a given PIO capability must be capable of supporting the minimum cycle time for that mode.
- If a drive does not report a PIO cycle time that is consistent with the Target PIO Cycle Time, a slower speed should be chosen.

6 Intel® ICH Timing Settings

6.1 Ultra DMA Timing Settings

When a drive will be operated in an Ultra DMA mode, the following table must be adhered to when programming the ICH ATA controller registers. NOTE: the following settings apply to Ultra DMA mode settings only.

Table 34. Ultra DMA Timing Value Based on Drive Mode

Intel® ICH Drive Mode	DMA Speed Used on DMA-Based Data Transfer Commands	UDMAC Value Ultra DMA Mode Enable Drive 0: bit 0 Drive 1: bit 1 Drive 2: bit 2 Drive 3: bit 3	UDMATIMx Value Ultra DMA CycleTime: Drive 0: bits 1:0 Drive 1: bits 5:4 Drive 2: bits 9:8 Drive 3: bits 13:12	IDE I/O Config Value For Cable Reporting: Drive 0: bit 4 Drive 1: bit 5 Drive 2: bit 6 Drive 3: bit 7	IDE I/O Config Value For 66MHz Base Clock: Drive 0: bit 0 Drive 1: bit 1 Drive 2: bit 2 Drive 3: bit 3	IDE I/O Config Value For 100MHz Base Clock: Drive 0: bit 12 Drive 1: bit 13 Drive 2: bit 14 Drive 3: bit 15
N/A (Ultra DMA Not Supported)	Non-Ultra DMA if supported	Disabled	Default	No Significance	0	0
Ultra DMA Mode 0	Ultra DMA Mode 0	Enabled	00b: CT=4 clks, RP=6 clks	No Significance	0	0
Ultra DMA Mode 1	Ultra DMA Mode 1	Enabled	01b: CT=3 clks, RP=5 clks	No Significance	0	0
Ultra DMA Mode 2	Ultra DMA Mode 2	Enabled	10b: CT=2 clks, RP=4 clks	No Significance	0	0
Ultra DMA Mode 3	Ultra DMA Mode 3	Enabled	01b: CT=3 clks, RP=8 clks	1[1]	1	0
Ultra DMA Mode 4	Ultra DMA Mode 4	Enabled	10b: CT=2 clks, RP=8 clks	1[2]	1	0
Ultra DMA Mode 5	Ultra DMA Mode 5	Enabled	01b: CT=1 clk, RP=16 clks	1[3]	0	1

NOTES:

1. This setting assumes an 80-conductor cable is present for the desired channel. Presence of a 40-conductor cable will limit a device to Ultra DMA mode 2 or less.
2. This setting assumes an 80-conductor cable is present for the desired channel. Presence of a 40-conductor cable will limit a device to Ultra DMA mode 2 or less.
3. This setting assumes an 80-conductor cable is present for the desired channel. Presence of a 40-conductor cable will limit a device to Ultra DMA mode 2 or less.

6.2 Multi-/Single-Word DMA and PIO Timing Settings

This section describes the desired controller configuration for PIO and/or multi-/single-word DMA modes of operation. Ultra DMA mode settings are completely independent of the following timings.

Table 35. Intel® ICH Drive Mode Based on DMA/PIO Capabilities

Drive's Best DMA Capability	Drive's Best PIO Capability	Intel® ICH Timing Mode	Fast PIO Supported? Best PIO Mode >= Best DMA Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	DMA Timing Enable Only Select (see note 1)	Pre-Fetch and Posting Enable Select	IORDY Sample Point Enable Select	Fast Timing Bank Drive Select
N/A (DMA not supported)	PIO0/1/ Compatible	Mode 0	No	No	Disabled	Enabled (if fixed disk)	Disabled	Disabled
N/A (DMA not supported)	PIO2	Mode 2	Yes	No	Disabled	Enabled (if fixed disk)	Depends on Drive	Enabled
N/A (DMA not supported)	PIO3 (w/IORDY)	Mode 3	Yes	No	Disabled	Enabled (if fixed disk)	Enabled	Enabled
N/A (DMA not supported)	PIO4 (w/IORDY)	Mode 4	Yes	No	Disabled	Enabled (if fixed disk)	Enabled	Enabled
Single-Word DMA Mode 2	PIO0/1/ Compatible	Mode 2	No (special config. needed)	Yes	Enabled	Enabled (if fixed disk)	Enabled	Enabled
Single-Word DMA Mode 2	PIO2	Mode 2	Yes	Yes	Enabled	Enabled (if fixed disk)	Enabled	Enabled
Single-Word DMA Mode 2	PIO3 (w/IORDY)	Mode 2	Yes	Yes	Enabled	Enabled (if fixed disk)	Enabled	Enabled
Single-Word DMA Mode 2	PIO4 (w/IORDY)	Mode 4	Yes	No	Disabled	Enabled (if fixed disk)	Enabled	Enabled
Multi-Word DMA Mode 1	PIO0/1/ Compatible/ PIO2	Mode 3	No (special config. needed)	Yes	Enabled	Enabled (if fixed disk)	Enabled	Enabled
Multi-Word DMA Mode 1	PIO3 (w/IORDY)/ PIO4 (w/IORDY)	Mode 3	Yes	Yes	Disabled	Enabled (if fixed disk)	Enabled	Enabled

Drive's Best DMA Capability	Drive's Best PIO Capability	Intel® ICH Timing Mode	Fast PIO Supported? Best PIO Mode >= Best DMA Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	DMA Timing Enable Only Select (see note 1)	Pre-Fetch and Posting Enable Select	IORDY Sample Point Enable Select	Fast Timing Bank Drive Select
Multi-Word DMA Mode 2	PIO0/1/ Compatible/ PIO2	Mode 4	No (special config. needed)	Yes	Enabled	Enabled (if fixed disk)	Enabled	Enabled
Multi-Word DMA Mode 2	PIO3 (w/IORDY)	Mode 4	Yes	Yes	Enabled	Enabled (if fixed disk)	Enabled	Enabled
Multi-Word DMA Mode 2	PIO4 (w/IORDY)	Mode 4	Yes	Yes	Disabled	Enabled (if fixed disk)	Enabled	Enabled

NOTES:
1. Configurations where a drive reports a PIO speed much slower than its reported DMA speed require the *DMA Timing Enable Only Select* bit to be Enabled.

Important rules:

1. Configurations where a drive reports a PIO speed much slower than its reported DMA speed require the *DMA Timing Enable Only Select* bit to be Enabled. The rule-of-thumb is when PIO is two speeds slower, so when multi-word -2 and PIO-2 are the fastest modes supported by a device, DMA-only is enabled with DTE bit set.
2. IORDY sample point enable (IE) bit is enabled if the operating mode is mode-2 or faster. The device must also support IORDY flow control in PIO mode-2 before setting this bit.
3. Pre-fetch/Posting enable bit shall be set if the operating mode is mode-2 or faster, but not if the device is an ATAPI device.
4. Fast Timing Bank enable shall be enabled if the operating mode is mode-2 or faster.
5. The operating mode shall be controlled by the device's PIO speed if the best PIO mode is 2 mode speeds faster than the DMA mode, or if below single-word-2 are supported by the device.

Table 36. IDE Drive Mode Register vs. Drive Feature Settings for Optimal DMA/PIO Operation

Intel® ICH IDE Drive 1 Mode Settings	ICH IDE Drive 0 Mode Settings	DMA Timing Enable Only Select 1	Pre-Fetch and Posting Enable Select 1	IORDY Sample Point Enable Select 1	Fast Timing Bank Drive Select 1	DMA Timing Enable Only Select 0 (see note 1)
Mode 0	Mode 4	Disabled	Disabled (mode < 2)	Disabled	Disabled	Depends on Drive
Not Present	Mode 4	Disabled	Disabled	Disabled	Disabled	Depends on Drive
Mode 2	Mode 4	Depends on Drive	Enabled (if fixed disk)	Depends on Drive	Enabled	Depends on Drive
Mode 3	Mode 4	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Depends on Drive
Mode 4	Mode 4	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Depends on Drive
Mode 0	Mode 3	Disabled	Disabled (mode < 2)	Disabled	Disabled	Depends on Drive
Not Present	Mode 3	Disabled	Disabled	Disabled	Disabled	Depends on Drive
Mode 2	Mode 3	Depends on Drive	Enabled (if fixed disk)	Depends on Drive	Enabled	Depends on Drive
Mode 3	Mode 3	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Depends on Drive
Mode 4	Mode 3	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Depends on Drive
Mode 0	Mode 2	Disabled	Disabled (mode < 2)	Disabled	Disabled	Depends on Drive
Not Present	Mode 2	Disabled	Disabled	Disabled	Disabled	Depends on Drive
Mode 2	Mode 2	Depends on Drive	Enabled (if fixed disk)	Depends on Drive	Enabled	Depends on Drive
Mode 3	Mode 2	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Depends on Drive
Mode 4	Mode 2	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Depends on Drive
Mode 0	Mode 0	Disabled	Disabled (mode < 2)	Disabled	Disabled	Disabled
Not Present	Mode 0	Disabled	Disabled	Disabled	Disabled	Disabled
Mode 2	Mode 0	Depends on Drive	Enabled (if fixed disk)	Depends on Drive	Enabled	Disabled
Mode 3	Mode 0	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Disabled
Mode 4	Mode 0	Depends on Drive	Enabled (if fixed disk)	Enabled	Enabled	Disabled

Table 36. IDE Drive Mode Register vs. Drive Feature Settings for Optimal DMA /PIO Operation, cont.

Intel® ICH IDE Drive 1 Mode Settings	ICH IDE Drive 0 Mode Settings	Pre-Fetch and Posting Enable Select 0	IORDY Sample Point Enable Select 0 (see note 2)	Fast Timing Bank Drive Select 0	IDE Timing Register Value bits 15:8 (hex) (see note 3) [all speeds]	Slave IDE Timing Register Value (hex) bits 3:0 (Primary) or bits 7:4 (Secondary) [all speeds]	IDE Timing Register Value bits 7:0 (binary)
Mode 0	Mode 4	Enabled (if fixed disk)	Enabled	Enabled	A3 (or E3)	0	0000xx11
Not Present	Mode 4	Enabled (if fixed disk)	Enabled	Enabled	A3 (or E3)	0	0000xx11
Mode 2	Mode 4	Enabled (if fixed disk)	Enabled	Enabled	E3	4	Xxx1xx11
Mode 3	Mode 4	Enabled (if fixed disk)	Enabled	Enabled	E3	9	Xx11xx11
Mode 4	Mode 4	Enabled (if fixed disk)	Enabled	Enabled	E3 (or A3)	B	Xx11xx11
Mode 0	Mode 3	Enabled (if fixed disk)	Enabled	Enabled	A1	0	0000xx11
Not Present	Mode 3	Enabled (if fixed disk)	Enabled	Enabled	A1	0	0000xx11
Mode 2	Mode 3	Enabled (if fixed disk)	Enabled	Enabled	E1	4	Xxx1xx11
Mode 3	Mode 3	Enabled (if fixed disk)	Enabled	Enabled	E1 (or A1)	9	Xx11xx11
Mode 4	Mode 3	Enabled (if fixed disk)	Enabled	Enabled	E1	B	Xx11xx11
Mode 0	Mode 2	Enabled (if fixed disk)	Depends on Drive	Enabled	90 (or D0)	0	0000xxx1
Not Present	Mode 2	Enabled (if fixed disk)	Depends on Drive	Enabled	90 (or D0)	0	0000xxx1
Mode 2	Mode 2	Enabled (if fixed disk)	Depends on Drive	Enabled	D0 (or 90)	4	Xxx1xxx1
Mode 3	Mode 2	Enabled (if fixed disk)	Depends on Drive	Enabled	D0	9	Xx11xxx1
Mode 4	Mode 2	Enabled (if fixed disk)	Depends on Drive	Enabled	D0	B	Xx11xxx1
Mode 0	Mode 0	Disabled (mode < 2)	Disabled	Disabled	80 (or C0)	0	00000000
Not Present	Mode 0	Disabled (mode < 2)	Disabled	Disabled	80 (or C0)	0	00000000
Mode 2	Mode 0	Disabled (mode < 2)	Disabled	Disabled	C0	4	Xxx10000
Mode 3	Mode 0	Disabled (mode < 2)	Disabled	Disabled	C0	9	Xx110000
Mode 4	Mode 0	Disabled (mode < 2)	Disabled	Disabled	C0	B	Xx110000

NOTES:
1. DMA Timing Enable Only field is in general disabled. It is only enabled in certain cases if the DMA Mode capability of the drive is much great than the PIO mode capability of the drive.
2. The IORDY Sample Point field must be enabled for PIO Modes 3 and 4. It is enabled on PIO2 drives if and only if IORDY capability is supported in the drive
3. The recommendations assume that if the attached slave drive is Mode 0 or not present, SITRE bit is 0.

6.3 Multi-/Single-Word DMA and PIO Timing Settings, Another Method

This section describes the desired controller configuration for PIO and/or multi-/single-word DMA modes of operation in a different manner than the previous section. Ultra DMA mode settings are completely independent of the following timings.

Note: The following settings apply to PIO, single-word and multi-word DMA mode settings only.

Table 37. DMA/PIO Timing Values Based on Intel® ICH Cable Mode/System Speed

Intel® ICH Drive Mode	IORDY Sample Point (ISP) bits 1:0	Recovery Time (RCT) bits 1:0	IDETIMx Value Drive 0 (Master) if Slave Attached bits 15:8	IDETIMx Value Drive 0 (Master) if no slave attached or slave is Mode 0[1] bits 15:8	SIDETIM Value Drive 1 (Slave) bits 3:0 (Primary) or bits 7:4 (Secondary)	Resultant Cycle Time (total clocks base operating freq)[2]
PIO0/ Compatible	Default	Default	C0h	80h	0	30 MHz: 900 ns 33 MHz: 900 ns
PIO2/SW2	4 clocks	4 clocks	D0h	90h	4	30 MHz: 256 ns 33 MHz: 240 ns
PIO3/MW1	3 clocks	3 clocks	E1h	A1h	9	30 MHz: 198 ns 33 MHz: 180 ns
PIO4/MW2	3 clocks	1 clock	E3h	A3h	B	30 MHz: 132 ns 33 MHz: 120 ns

NOTES:
1. The table assumes that if the attached slave drive is Mode 0 or not present, the SITRE bit is 0.
2. The table assumes that 25 MHz is not supported as a target PCI system speed. If the DMA Timing Enable Only (DTE) bit has been enabled for that drive, this resultant cycle time applies to data transfers performed with DMA only.

7 Drive Configuration for Selected Timings

Once the ICH timing modes for DMA, PIO and Ultra DMA have been selected, the Set Features Command (0xEF) with set transfer mode (subcommand 0x03) can be issued to set the drives on the system to the optimal speeds:

Table 38. Ultra DMA/Multi-Word DMA/Single-Word Transfer "Set Features" Mode Values

Drive's Selected Ultra DMA Capability	Drive's Selected non-Ultra DMA Capability	Selected Speed	ATA "SET FEATURES" Command Set Transfer Mode Sub Command Parameter for selected speed
Ultra DMA Mode 5	N/A	Ultra DMA Mode 5	45h
Ultra DMA Mode 4	N/A	Ultra DMA Mode 4	44h
Ultra DMA Mode 3	N/A	Ultra DMA Mode 3	43h
Ultra DMA Mode 2	N/A	Ultra DMA Mode 2	42h
Ultra DMA Mode 1	N/A	Ultra DMA Mode 1	41h
Ultra DMA Mode 0	N/A	Ultra DMA Mode 0	40h
N/A	Multi-Word DMA Mode 2	Multi-Word DMA Mode 2	22h
N/A	Multi-Word DMA Mode 1	Multi-Word DMA Mode 1	21h
N/A	Single-Word DMA Mode 2	Single-Word DMA Mode 2	12h
N/A	N/A	Disabled	N/A

Refer to the Set Features Command description in the ATA Specification for more information.

Table 39. PIO Transfer/Mode Values

Drive's Selected PIO Speed Capability	ATA "SET FEATURES" Command Set Transfer Mode Sub Command Parameter for Selected Speed
PIO0/PIO1/PIO2/Compatible	N/A
PIO3 w/IORDY Flow Control	C3
PIO4 w/IORDY Flow Control	C4

A drive may only be enabled for one Single DMA capability (mode). In general, if a drive supports an Ultra DMA speed, then the drive shall be configured for Ultra DMA. If a drive does not support Ultra DMA, then it should be configured with its supported DMA speed, if it exists. If a drive supports only PIO (does not have support for either Ultra DMA or DMA speeds), then the drive shall only be accessed in a PIO mode only.

If a drive is configured for an Ultra DMA speed or a DMA speed, its corresponding DMA-capable bit in the “PCI Bus Master I/O Status Register” (Primary: PCI Bus Master IDE I/O Offset + 02h; Secondary - PCI Bus Master I/O Offset + 0Ah) MUST be set. This will allow DMA-capable device drivers to recognize the fact that this drive has been identified and configured by the BIOS for Ultra DMA operation.

8 Settings Checklist

The following checklists can be used in determining drive modes. Refer to the "Determining a Drive's Transfer Rate Capabilities" and "ICH Timing Settings" sections for more information.

Table 40. Drive Capabilities Checklist

Drive	Type (ATA Fixed Disk or ATAPI)	Position	Best Ultra DMA Mode (Ultra DMA Mode 0, 1, 2, or N/A)	Best DMA Mode (Single-Word 2, Multi-Word 1, 2, or N/A)	Best PIO Mode (Fast PIO Mode 2, 3, 4 or Compatible)	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode	80-Conductor Cable Present
Drive 0		Primary Master								
Drive 1		Primary Slave								
Drive 2		Secondary Master								
Drive 3		Secondary Slave								

Table 41. Intel® ICH Settings Checklist

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh		
PCI Bus Master IDE Base I/O Address	PCI	20–23h		Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40–41h		
IDE Timing Register 2	PCI	42–43h		
Secondary IDE Timing Register	PCI	44h		
Ultra DMA Control Register	PCI	48h		
Ultra DMA Timing Register	PCI	4A–4Bh		
IDE I/O Configuration	PCI	54–-55h		Ensure that bit 10 (of register value) is a 1, Ensure bits 4:7 (of register value) are 1 if an 80-conductor cable is present for each device. Ensure bits 0:3 (of register value) are 1 only when Ultra DMA mode 3 or 4 is selected and an 80-conductor cable is present for each device. Ensure bits x:x (of register value) are 1 only when Ultra DMA mode 5 is selected and an 80-conductor cable is present for each device.

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9 Example Configurations

This section provides examples of drive configurations on an ICH-based system.

9.1 Example #1: Ultra ATA/100 (Ultra DMA mode 5) Configuration

Table 42. UDMA Mode 5 Configuration

Drive	Type	Position	Cable Reporting	Best Ultra DMA Mode	Best DMA Mode	Best PIO Mode	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode
Drive 0	Fixed Disk	Primary Single	1 (80-conductor)	Ultra DMA Mode 5	Multi-Word DMA Mode 2	PIO 4	Ultra DMA Mode 5	Mode 4	Yes	Yes
Drive 2	ATAPI CDROM	Secondary Single	0 (40-conductor)	Ultra DMA Mode 4	Multi-Word DMA Mode 1	PIO 3	Ultra DMA Mode 2	Mode 3	Yes	Yes

In the above configuration, even though both drives support either Ultra ATA/100 or Ultra ATA/66, Ultra DMA may **not** be enabled on both of the drives: Ultra DMA mode 5 will be selected for Drive 0, however Ultra DMA mode 2 for Drive 2 since a 40-conductor cable is present. Fast PIO support will be enabled on each drive as well.

Table 43. UDMA Mode 5 Configuration (Cont.)

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh	System dependent	
PCI Bus Master IDE Base I/O Address	PCI	20–23h	System dependent	Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40–41h	A307h	Mode config. for Primary
IDE Timing Register 2	PCI	42–43h	A303h	Mode config. for Secondary
Secondary IDE Timing Register	PCI	44h	00h	
Ultra DMA Control Register	PCI	48h	05h	Drive 0 and 2 are Ultra DMA capable.
Ultra DMA Timing Register	PCI	4A–4Bh	0102h	Ultra DMA mode config.
IDE I/O Configuration Register	PCI	54–55h	0411h	Ultra DMA Clock & cable config, plus PIO Ping-Pong enable.

9.2 Example #2: Ultra ATA/66 (Ultra DMA mode 4) Configuration

Table 44. UDMA Mode 4 Configuration

Drive	Type	Position	Cable Reporting	Best Ultra DMA Mode	Best DMA Mode	Best PIO Mode	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode
Drive 0	Fixed Disk	Primary Single	1 (80-conductor)	Ultra DMA Mode 4	Multi-Word DMA Mode 2	PIO4	Ultra DMA Mode 4	Mode 4	Yes	Yes
Drive 2	ATAPI CDROM	Secondary Single	0 (40-conductor)	Ultra DMA Mode 3	Multi-Word DMA Mode 1	PIO3	Ultra DMA Mode 2	Mode 3	Yes	Yes

In the above configuration, even though both drives support Ultra DMA/66, Ultra DMA may **not** be enabled on each of the drives: Ultra DMA/66 mode 4 will be selected for Drive 0, however Ultra DMA mode 2 for Drive 1 since a 40-conductor cable is present. Fast PIO support will be enabled on each drive as well.

Table 45. UDMA Mode 4 Configuration (Cont.)

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh	System dependent	
PCI Bus Master IDE Base I/O Address	PCI	20–23h	System dependent	Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40–41h	A307h	Mode config. for Primary
IDE Timing Register 2	PCI	42–43h	A303h	Mode config. for Secondary
Secondary IDE Timing Register	PCI	44h	00h	
Ultra DMA Control Register	PCI	48h	05h	Drive 0 and 2 are Ultra DMA capable.
Ultra DMA Timing Register	PCI	4A–4Bh	0102h	Ultra DMA mode config.
IDE I/O Configuration Register	PCI	54–55h	0411h	Ultra DMA Clock & cable config, plus PIO Ping-Pong enable.

9.3 Example #3: Ultra ATA/33 Configuration

Table 46. UDMA Mode 3 Configuration

Drive	Type	Position	Best Ultra DMA Mode	Best DMA Mode	Best PIO Mode	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode
Drive 0	Fixed Disk	Primary Single	Ultra DMA Mode 2	Multi-Word DMA Mode 2	PIO4	Ultra DMA Mode 2	Mode 4	Yes	Yes
Drive 2	ATAPI CDROM	Secondary Single	Ultra DMA Mode 1	Multi-Word DMA Mode 1	PIO3	Ultra DMA Mode 1	Mode 3	Yes	Yes

In the above configuration, since both drives support Ultra DMA, Ultra DMA will be enabled on each of the drives: Ultra DMA mode 2 for Drive 0 and Ultra DMA mode 1 for Drive 1. Non-Ultra DMA and Fast PIO support will be enabled on each drive as well.

Table 47. UDMA Mode 3 Configuration (Cont.)

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh	System dependent	
PCI Bus Master IDE Base I/O Address	PCI	20–23h	System dependent	Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40–41h	A307h	Mode config. for Primary
IDE Timing Register 2	PCI	42–43h	A303h	Mode config. for Secondary
Secondary IDE Timing Register	PCI	44h	00h	
Ultra DMA Control Register	PCI	48h	05h	Drive 0 and 2 are Ultra DMA capable.
Ultra DMA Timing Register	PCI	4A–4Bh	0102h	Ultra DMA mode config.
IDE I/O Configuration Register	PCI	54–55h	0400h	Ultra DMA Clock & cable config, plus PIO Ping-Pong enable.

9.4 Example #4: Mixed Ultra ATA/66 and non-Ultra ATA/33 Configuration

Table 48. Mixed UDMA Mode 4 + Multi-Word-2 Configuration

Drive	Type	Position	Cable Reporting	Best Ultra DMA Mode	Best DMA Mode	Best PIO Mode	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode
Drive 0	Fixed Disk	Primary Master	1 (80-conductor)	Ultra DMA Mode 4	Multi-Word DMA Mode 2	PIO4	Ultra DMA Mode 4	Mode 4	Yes	Yes
Drive 1	Fixed Disk	Primary Slave	0 (40-conductor)	N/A	Multi-Word DMA Mode 2	PIO4	N/A (Ultra DMA disabled)	Mode 4	Yes	Yes
Drive 2	ATAPI CDROM	Secondary Single	0 (40-conductor)	N/A	Multi-Word DMA Mode 1	PIO3	N/A (Ultra DMA disabled)	Mode 3	Yes	Yes

In the above configuration, Ultra DMA mode 4 will only be enabled on Drive 0. Non-Ultra DMA and Fast PIO support will be enabled on each drive as well.

Table 49. Mixed UDMA Mode 4 + Multi-Word-2 Configuration (Cont.)

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh	System dependent	
PCI Bus Master IDE Base I/O Address	PCI	20–23h	System dependent	Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40—41h	E377h	Mode config. for Primary
IDE Timing Register 2	PCI	42–43h	A103h	Mode config. for Secondary
Secondary IDE Timing Register	PCI	44h	0Bh	
Ultra DMA Control Register	PCI	48h	01h	Drive 0 is Ultra DMA capable
Ultra DMA Timing Register	PCI	4A–4Bh	0002h	Ultra DMA mode config.
IDE I/O Configuration Register	PCI	54–55h	0411h	Ultra DMA Clock and cable config, plus PIO Ping-Pong enable

9.5 Example #5: Mixed Ultra ATA/33 and Non-Ultra ATA/33 Configuration

Table 50. Mixed UDMA Mode 3 + Multi-Word-2 Configuration

Drive	Type	Position	Best Ultra DMA Mode	Best DMA Mode	Best PIO Mode	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode
Drive 0	Fixed Disk	Primary Master	Ultra DMA Mode 2	Multi-Word DMA Mode 2	PIO4	Ultra DMA Mode 2	Mode 4	yes	yes
Drive 1	Fixed Disk	Primary Slave	N/A	Multi-Word DMA Mode 2	PIO4	N/A (Ultra DMA disabled)	Mode 4	yes	yes
Drive 2	ATAPI CDROM	Secondary Single	N/A	Multi-Word DMA Mode 1	PIO3	N/A (Ultra DMA disabled)	Mode 3	yes	yes

In the above configuration, Ultra DMA mode 2 will only be enabled on Drive 0. Non-Ultra DMA and Fast PIO support will be enabled on each drive as well.

Table 51. Mixed UDMA Mode 3 + Multi-Word-2 Configuration (Cont.)

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh	System dependent	
PCI Bus Master IDE Base I/O Address	PCI	20–-23h	System dependent	Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40–41h	E377h	Mode config. for Primary
IDE Timing Register 2	PCI	42–43h	A103h	Mode config. for Secondary
Secondary IDE Timing Register	PCI	44h	0Bh	
Ultra DMA Control Register	PCI	48h	01h	Drive 0 is Ultra DMA capable.
Ultra DMA Timing Register	PCI	4A–4Bh	0002h	Ultra DMA mode config.
IDE I/O Configuration Register	PCI	54–55h	0400h	Ultra DMA Clock and cable config, plus PIO Ping-Pong enable.

9.6 Example #6: Non Ultra ATA/33 Drive Configuration

Table 52. Multi-Word-2 Configuration

Drive	Type	Position	Best Ultra DMA Mode	Best DMA Mode	Best PIO Mode	Intel® ICH Ultra DMA Mode	ICH Mode	Non Ultra DMA Supported? Best DMA Mode is {SW2, MW1, MW2}	Fast PIO Supported? Best PIO Mode >= Best DMA Mode
Drive 0	Fixed Disk	Primary Master	N/A	Multi-Word DMA Mode 2	PIO4	N/A (Ultra DMA disabled)	Mode 4	yes	yes
Drive 1	Fixed Disk	Primary Slave	N/A	Multi-Word DMA Mode 2	PIO4	N/A (Ultra DMA disabled)	Mode 4	yes	yes
Drive 2	ATAPI CDROM	Secondary Single	N/A	Multi-Word DMA Mode 1	PIO3	N/A (Ultra DMA disabled)	Mode 3	yes	yes

In the above configuration, none of the drives supports Ultra DMA. Only Non-Ultra DMA and Fast PIO support will be enabled on each drive.

Table 53. Multi-Word-2 Configuration (Cont.)

Register	Type	Offset	Value	Comments
PCI Command Register	PCI	04h	0005h	Ensure that bits 0 and 2 are 1.
PCI Master Latency Timer	PCI	0Dh	System dependent	
PCI Bus Master IDE Base I/O Address	PCI	20–23h	System dependent	Ensure that bit 0 (of register value) is 1.
IDE Timing Register 1	PCI	40–41h	E377h	Mode config. for Primary
IDE Timing Register 2	PCI	42–43h	A103h	Mode config. for Secondary
Secondary IDE Timing Register	PCI	44h	0Bh	
Ultra DMA Control Register	PCI	48h	00h	Ultra DMA is disabled for all drives.
Ultra DMA Timing Register	PCI	4A–4Bh	0000h	
IDE I/O Configuration Register	PCI	54–55h	0400h	Ultra DMA Clock & cable config, plus PIO Ping-Pong enable.

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10 System Software Considerations for the Intel® ICH Family

This section outlines some of the key system considerations for systems using the Ultra ATA Controller.

10.1 Ultra DMA System Software Considerations

This section outlines some of the key system considerations for systems where Ultra DMA operation is enabled.

The following components shall comprise an Ultra ATA/100 System:

1. Ultra ATA/100-capable Host ATA Controller
2. Ultra ATA/100-capable ATA/ATAPI Devices
3. Ultra ATA/100 Aware BIOS and /or System Initialization Software
4. Ultra ATA/100 Aware Device Driver

Two of the aforementioned components are software based with specific requirements: Item #3, Ultra ATA/100 Aware BIOS and/or System Initialization Software; and Item #4, Ultra ATA/100 Aware Device Driver having the following attributes.

Ultra ATA/100 Aware BIOS and/or System Initialization Software shall:

1. Identify Ultra DMA capable devices and host controllers.
2. Identify 80-conductor versus 40-conductor cable presence for each device, reporting the information into the “IDE I/O Configuration” register. Note, presence of the 40-conductor cable shall result in limiting operation to Ultra DMA mode 2 (or less), which follows the Ultra ATA/33 specification.
3. Configure Ultra ATA/100 operation for all Ultra ATA/100 capable devices and host controllers.
4. Preserve Ultra ATA/100 configuration across reset states, restoring Ultra ATA/100 operation (described in Item #3) as necessary.

Ultra ATA/100 Aware Device Drivers shall:

1. Provide support for "PCI Bus Master IDE" Operation (SFF8038i)
    a) Identify system configured for DMA operation.
        i. Identify DMA and Ultra ATA/(100, 66 or 33) capable devices and host controllers.
        ii. Utilize DMA when it determines that Host Controller and ATA/ATAPI devices have fulfilled device driver-specific, configuration requirements for DMA operation.
        iii. Read IDE I/O Configuration "Cable Reporting" bits (set by BIOS) to determine if Ultra ATA/100 is acceptable when an 80-conductor cable is present, or to limit to Ultra ATA/33 speeds when 40-conductor cable is present.
    b) Perform data transfer commands with DMA on devices, host controllers that support DMA
2. Provide recovery for data transfers that fail as the result of Ultra ATA/100 interface CRC errors:
    a) Determine that the data transfer command's error source is an Ultra DMA interface CRC error.
    b) Retry data transfer command when an Ultra DMA interface CRC is the source of an error.
3. Ensure that the Ultra ATA/100 configuration of the devices and host controller is restored when events that clear the Ultra ATA/100 enabled status are encountered.

- Ensure that Hard Resets are never issued to the device during a power cycle

or

- Provide path to Ultra ATA/100 Aware BIOS and/or System Initialization Software in the case of a Hard/Power-On reset.

When enabled on the host controller and devices, Ultra DMA operation shall be used for all data transfer commands issued by the Ultra DMA Aware Device Driver. PIO or multi-word DMA shall be the mode of access used with devices and host controllers that do not support Ultra DMA modes of operation.

10.2 General Device Driver Considerations

This section provides information regarding Terminating Transfers performed with Ultra ATA/100 and DMA device drivers or system software.

In normal DMA operations, at the end of a data transfer, the ATA device signals an interrupt. In response to the interrupt, software verifies that the bus is idle and then writes the Stop Bus Master Command. It then reads the controller status register to determine if the transfer completed

successfully. For a detailed description of the "Bus Master IDE Status" Register refer to the section of this document called "*Bus Master IDE Command and Status Register.*"

If the ATA device does not signal completion of a command by an interrupt, the bus master transfer did not complete successfully. In this case, it is necessary to read the "Bus Master IDE Status" Register to check if the bus is idle or active. If the bus is active it is necessary to send the "Stop Bus Master" Command and reset the ATA controller and drives connected to the ATA cable prior to sending out the next ATA/ATAPI drive command to the cable. This is necessary because the cable (Primary or Secondary ATA) may not be ready to receive new commands unless the DMA state machine has stopped. All the drives on the cable should be reset.

In general, a prematurely terminated command on the ATA bus implies that some of the state machines in the drive and/or in the ATA controller are still in an "active" condition. By performing a drive reset immediately following the burst "stop", the ICH will be in a state such that the ATA DMA engines can be programmed to perform the transfer once again.

When configuring for Ultra DMA modes, the UDMATIM register and IDE I/O Configuration registers must work in concert to effectively set up the ICH.

10.3 Ultra DMA Cable Detection Considerations

The cable detection mechanism for Ultra ATA/100 is a requirement that must be dealt with by the BIOS. Specified by this document (when using the ICH5, ICH4, ICH3, ICH2 or ICH), the absence or presence of an 80-conductor cable must be determined by some method and indicated in the "IDE PCI Configuration" Register (offset 54h, bits4-7) for use in higher level OS drivers. While this method is to be platform (hardware + BIOS) specified, two choices exist:

1. Implement cable detection through system hardware by implementing the detection method specified in the X3T13 technical committee's ATA-4 specification. This method requires the system BIOS to use GPIO hardware to detect the cable type.
2. Implement cable detection through the method specified in the AT Attachment with Packet Interface – 6 (ATA/ATAPI-6) specification, which has the device detect the cable type and reports the absence or presence of the 80-conductor cable through the Identify Drive command. Note that this method requires the system hardware manufacturer to include a single capacitor on the motherboard ATA connector. Please review the AT Attachment with Packet Interface – 6 (ATA/ATAPI-6) specification for proper placement, size and usage of this capacitor, plus the proper reporting methods for the ATA drives.

Both methods listed have their own possibilities of incorrect indication of cable type, but simultaneous use of both methods result in a higher likelihood of indicating the correct cable type. It is suggested to use both methods, with an 80-conductor cable indication reported when both methods agree that an 80-conductor cable exists.

10.4 Power Management Software Considerations

ACPI-Capable BIOS must prepare ASL codes that the OS ACPI drivers (e.g. Microsoft* Windows* 98 ACPI.SYS) will use to reconfigure the system. The ACPI BIOS must indicate how the ATA controller PCI configuration space must be re-configured, plus indicate how to reconfigure the drives after resuming from the S3 power state.

The ACPI BIOS must program the drive (on the cable) and controller to identical settings, or risk the possibility of resume data errors on the drive. Because users may add older hardware, the ACPI BIOS must not hard-code the drive reconfiguration ASL codes that translate into "Set Features" commands that are sent to the drive. Hard coding ASL codes to Ultra DMA mode 2 when the drive is originally set to Ultra DMA mode 5 will result in data corruption.

10.5 Bus Master IDE Command and Status Register

BMICX—BUS MASTER IDE COMMAND REGISTER (IO)

Address Offset: Primary Channel—Base + 00h; Secondary Channel—Base + 08h
Default Value: 00h
Attribute: Read/Write

This register enables/disables bus master capability for the ATA function and provides direction control for the ATA DMA transfers. This register also provides bits that software uses to indicate DMA capability of the ATA device.

This register enables/disables bus master capability for the ATA function and provides direction control for the ATA DMA transfers. This register also provides bits that software uses to indicate DMA capability of the ATA device.

Table 54. Bus Master IDE Command Register

Bit	Description
7:4	**Reserved.**
3	**Bus Master Read/Write Control (RWCON).** 0=Reads; 1=Writes. This bit must NOT be changed when the bus master function is active. While a Ultra DMA transfer is in progress, this bit will be READ ONLY. The bit will return to read/write once the synchronous DMA transfer has been completed or halted.
2:1	**Reserved.**
0	**Start/Stop Bus Master (SSBM).** 1=Start; 0=Stop. When this bit is set to 1, bus master operation starts. The controller transfers data between the ATA device and memory only while this bit is set. Master operation can be stopped by writing a 0 to this bit. This results in all state information being lost (i.e., master mode operation cannot be stopped and then resumed). If this bit is set to 0 while bus master operation is still active (i.e., Bit 0=1 in the Bus Master IDE Status Register for that ATA channel) and the drive has not yet finished its data transfer (bit 2=0 in the channel's Bus Master IDE Status Register), the bus master command is aborted and data transferred from the drive may be discarded by ICH rather than being written to system memory. This bit is intended to be set to 0 after the data transfer is completed, as indicated by either bit 0 or bit 2 being set in the ATA Channel's Bus Master IDE Status Register.

BMISX—BUS MASTER IDE STATUS REGISTER (IO)

Address Offset: Primary Channel—Base + 02h; Secondary Channel—Base + 0Ah
Default Value: 00h
Attribute: Read/Write Clear

This register provides status information about the ATA device and state of the ATA DMA transfer.

Table 55. Bus Master IDE Status Register

Bit	Description
7	**Reserved.** This bit is hardwired to 0.
6	**Drive 1 DMA Capable (DMA1CAP)—R/W.** 1=Drive 1 is capable of DMA transfers. This bit is a software controlled status bit that indicates ATA DMA device capability and does not affect hardware operation.
5	**Drive 0 DMA Capable (DMA0CAP)—R/W.** 1=Drive 0 is capable of DMA transfers. This bit is a software controlled status bit that indicates ATA DMA device capability and does not affect hardware operation.
4:3	**Reserved.**
2	**IDE Interrupt Status (IDEINTS)—R/WC.** This bit, when set to a 1, indicates when an ATA device has asserted its interrupt line. When bit 2=1, all read data from the ATA device has been transferred to main memory and all write data has been transferred to the ATA device. Software sets this bit to a 0 by writing a 1 to it. IRQ14 is used for the primary channel and IRQ15 is used for the secondary channel. Note that, if the interrupt status bit is set to a 0 by writing a 1 to this bit while the interrupt line is still at the active level, this bit remains 0 until another assertion edge is detected on the interrupt line.
1	**IDE DMA Error—R/WC.** This bit is set to 1 when ICH encounters a target abort or master abort while transferring data on the PCI Bus. Software sets this bit to a 0 by writing a 1 to it.
0	**Bus Master IDE Active (BMIDEA)—RO.** ICH sets this bit to 1 when bit 0 in the BMICx Register is set to 1. ICH sets this bit to 0 when the last transfer for a region is performed (where EOT for that region is set in the region descriptor). ICH also sets this bit to 0 when bit 0 of the BMICx Register is set to 0. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.

Table 56. Interrupt/Activity Status Combinations

Bit 2	Bit 0	Description
0	1	**DMA transfer is in progress.** The ATA device has generated no interrupt.
1	0	**The IDE device generated an interrupt and the Physical Region Descriptors exhausted.** This is normal completion where the size of the physical memory regions is equal to the ATA device transfer size.
1	1	**The IDE device generated an interrupt.** The controller has not reached the end of the physical memory regions. This is a valid completion case when the size of the physical memory regions is larger than the ATA device transfer size.
0	0	**Error condition.** If the IDE DMA Error bit is 1, there is a problem transferring data to/from memory. Specifics of the error have to be determined using bus-specific information. If the Error bit is 0, the PRD specified a smaller buffer size than the programmed DMA transfer size.

10.6 Native PCI Mode Considerations

The ICH5, ICH4 and ICH3 ATA controllers have the ability to be programmed for either Compatibility or Native PCI. The term Compatibility indicates use of fixed legacy resources, and the term Native PCI indicates use of plug-and-play resources that are all programmable through the ICH5, ICH4 and ICH3 ATA controller's PCI configuration registers.

The ICH5, ICH4 and ICH3 ATA controller's default state is compatibility mode, so the programming interface register will have the value of "0x0A." The Base Address Registers for task file access (BAR0-3) will not be programmable at this point, showing the default value of 0.

If Native PCI operation is desired, each device can be independently enabled into this mode of operation by writing a 1 into its associated mode enable bit in the Programming Interface PCI configuration register. It is advised that both Primary and Secondary controllers are put in the same mode of operation. To program both controllers for Native PCI operation, the Programming Interface register must be written with the value of "0x0F". At this time, the BAR0-3 will show the value of "0x00000001". These BARs are I/O base addresses, which can be assigned anywhere in the IA-32 64k-addressable I/O space.

During the Compatibility to Native PCI switch, drivers that access the ATA controller must not access the task file registers by either the legacy or native addresses. When the controller is in Compatibility mode, the BAR0-3 based I/O addresses must not be used for task-file accesses. Conversely, when the controller is in the Native PCI mode, the legacy I/O addresses must not be used for task-file accesses.

Now all the BARs in the ATA controller's PCI configuration space must be programmed according to the *PCI Local Bus Specification, Revision 2.3*, after which the Command register's Memory and I/O space enable bits must both be set to 1. Early enabling of the Memory and I/O space enable bits will cause undesirable responses.

The BIOS must be able to support Native PCI mode.

10.7 Intel® ICH5, ICH4 and ICH3 Specification Considerations

The ICH5, ICH4 and ICH3 have an Expansion Base Memory Address Register, which requires a 1-Kbyte DWORD aligned memory space. This space is Intel reserved for future functionality.