Intel® 815E Chipset Platform for Use with Universal Socket 370

Design Guide Update

October 2002

Notice: The Intel® 815E chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 298594-007

Contents

Revision History

Revision.	Draft/Changes	Date
-001	Initial Release	October 2001
-004	Revision Number corrected to –004 due to numbering error. Added Documentation Changes #9 - #16	January 2002
-005	Added Document Change #17, changed Section 13.3.3, 3.3V/V5REF Sequencing	March 2002
-006	Added Document Change #18-19.	April 2002
-007	Added Schematic, Layout and Routing Change #6	October 2002

Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® 815E Chipset Platform for Use with Universal Socket 370 Design Guide*, Document #298350-002, dated September 2002. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2000. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public update document when the public document is first published. This update document contains a complete list of all known information types.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 815E Chipset Platform for Use with Universal Socket 370 Design Guide, September 2002	298350-002

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815E Chipset Platform for Use with Universal Socket 370.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	Added Support for P-MOS Kicker “ON”: SMAA[9] Is Strapped High by Internal 50 kΩ Pull-Up

NO.	Plans	SCHEMATIC, LAYOUT AND ROUTING UPDATES
1	Doc	Changed: Appendix A, Schematic Page 7 of 33, Replace PR42
2	Doc	Changed: Appendix A, Schematic Page 27 of 33, Replace R390 and R393
3	Doc	Changed: Appendix A, Schematic Page 29 of 33, Change R394 and R395 Connections
4	Doc	Changed: Appendix A, Schematic Page 26 of 33, Change VTTPWRGD Circuit
5	Doc	Changed: Appendix A, Schematic Page 7 of 33, Change SMAA[9] Circuit to Enable FSB P-MOS Kicker
6	Doc	Changed: Appendix A, Schematic Page 7 of 33, Delete SM_BS0, SM_BS1

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Added: Workaround for THERMTRIP Erratum
2	Doc	Corrected: Checklist Item Figure Number in Section 14.4.12, RTC
3	Doc	Changed: Processor Pin Names, Section 5.4
4	Doc	Changed: Processor Pin Names, Section 4.1
5	Doc	Changed: Added Information and Figure to Section 11.8.6, Power-Well Isolation Control Strap Requirements
6	Doc	Changed: Section 14.4.9, Power Management; Modified
7	Doc	Changed: Section 1.3.2.1, Intel® 82815 GMCH Features, Packaging/Power; Bullet Modified
8	Doc	Changed: Figure 100, Power Delivery Map; Replaced
9	Doc	Added Section 10.5 Power_Supply PS_ON Considerations
10	Doc	Changed Section 14.4.12, RTC, Add SUSCLK to the Checklist
11	Doc	Changed Section 14.4.15, Power, Modify Checklist Recommendations for 5V_REF_SUS
12	Doc	Changed Section 13.3.3, 3.3V/V5REF Sequencing
13	Doc	Changed Figure 86, Trace Routing, in Section 11.9.2.1, General Trace Routing Considerations

NO.	Plans	DOCUMENTATION CHANGES
14	Doc	Changed Figure 81-a, RTC Power Well Isolation Control, in Section 11.8.6, Power Well Isolation Control Strap Requirements
15	Doc	Changed Table 39, Intel® CK-815 (2-DIMM) Clocks, in Section 12.1, 2-DIMM Clocking
16	Doc	Changed Table 40, Intel® CK-815 (3-DIMM) Clocks, in Section 12.2, 3-DIMM Clocking
17	Doc	Changed Section 13.3.3, 3.3V/V5REF Sequencing
18	Doc	Changed Figure 100, Power Delivery Map, in Section 13, Power Delivery
19	Doc	Added Section 2.2, Electrostatic Discharge Platform Recommendations

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General Design Considerations

1. Added Support for P-MOS Kicker “ON”: SMAA[9] Is Strapped High by an Internal 50 kΩ Pull-Up

The PSB P-MOS Kicker circuit should be enabled (SMAA[9] is strapped high through an internal 50 kΩ pull-up resistor to enable P-MOS Kicker) on all new, future 815E Universal Socket 370 designs. Use of the P-MOS Kicker circuit improves PSB timings by improving AGTL and AGTL+ signal flight time.

Existing designs which have implemented the pull-down resistor circuit on the SMAA[9] signal as shown in the Customer Reference Board schematics and populated the resistor site to over-ride the internal pull-up resistor, may depopulate the site to enable the P-MOS Kicker circuit. This activity should be based on timing analysis of the specific platform.

P-MOS Kicker circuit “ON” is the recommended setting for 815E Universal Socket 370 designs using future 0.13 micron technology processors

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Schematic, Layout and Routing Updates

1. Changed: Appendix A, Schematic Page 7 of 33, Replace PR42

The GTLREF circuit for the GMCH does not reflect the updated recommendation in the design guide. Resistor PR42 should be replaced with a 63.4 kΩ, 1% resistor.

2. Changed: Appendix A, Schematic Page 27 of 33, Replace R390 and R393

With the change in the VRM specification for the Intel® Pentium® III processor 900 MHz, the reference schematic has been updated to meet that processor's load line requirements. Resistor R390 should be replaced with a 27.4 kΩ, 1% resistor. Resistor R393 should be replaced with a 30.1 kΩ, 1% resistor.

3. Changed: Appendix A, Schematic Page 29 of 33, Change R394 and R395 Connections

The reference schematics do not reflect the proper implementation of the BSEL signals. Resistor R394 should be connected to FMOD1 instead of FMOD0. Resistor R395 should be connected to FMOD0 instead of FMOD1.

4. Changed Appendix A, Schematic Page 26 of 33, Change VTTPWRGD Circuit

To guarantee proper operation of the comparators in the VTTPWRGD circuit, the power rail of U32 should be connected to 5-V standby instead of normal VCC5.

5. Changed Appendix A, Schematic Page 7 of 33, Change SMAA[9] Circuit to Enable FSB P-MOS Kicker

To enable the front side bus P-MOS Kicker, remove R88. The SMAA[9] signal has an internal 50 kΩ pull-up which enables the P-MOS Kicker at power-up.

6. Changed Appendix A, Schematic Page 7 of 33, Delete SM_BS0, SM_BS1

SM_BS0 and SM_BS1 are reserved pins, therefore the circuit shown on page 7 of 33 should be deleted along with the Table references to SM_BS0/SM_BS1.

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Documentation Changes

1. Addition of Workaround for THERMTRIP Erratum

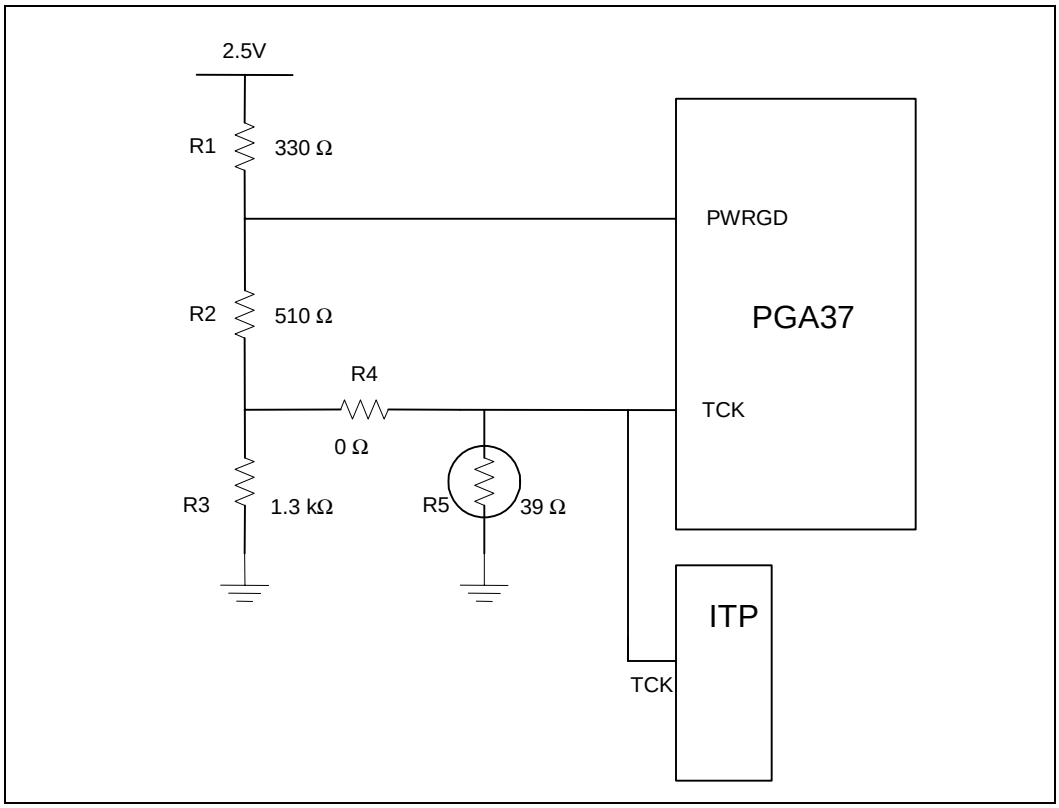
Reference Section 5.3.1, THERMTRIP Circuit, page 57. The following text has been added to the end of the section as Section 5.3.1.2, THERMTRIP Support for Tualatin A-1 Stepping:

> A platform supporting the 0.13 micron technology processor must implement a workaround required for the A-1 stepping of that processor, identified by CPUID = 6B1h.
>
> The internal control register bit responsible for operation of the THERMTRIP circuit functionality may power up in an un-initialized state. As a result, THERMTRIP# may be incorrectly asserted during de-assertion of RESET# at nominal operating temperatures. When THERMTRIP# is asserted as a result of this, the processor may shut down internally and stop execution. In addition, when the THERMTRIP# pin is asserted the processor may incorrectly continue to execute, leading to intermittent system power-on boot failures. The occurrence and repeatability of failures is system dependent, however all systems and processors are susceptible to failure.
>
> To prevent the risk of power-on boot failures, a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:
>
> - •Rising edge occurs after Vcc_core is valid and stable
> - •Rising edge occurs before or at the de-assertion of RESET#
> - •Rising edge occurs after all Vref input signals are at valid voltage levels
> - •TCK input meets the Vih min (1.3 V) and max (1.65 V) spec requirements

Specific workaround implementations may be platform specific. The following examples have been tested as acceptable workaround implementations.

Note: The example workaround circuits attached require circuit modification for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Review the accompanying notes with each workaround for ITP modification details. If the system fails to boot when using ITP, issuing the ITP ‘Reset Target’ command on failing systems will reset the system and provide a sufficient rising edge on the TCK pin to ensure proper system boot.

In addition, the example workaround circuits shown do not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.



For Production Boards:
Depopulate R5

To use ITP:
Install R5, Depopulate R4

2. Corrected: Checklist Item Figure Number in Section 14.4.12, RTC

The following checklist item figure number is corrected in Section 14.4.12, *RTC*:

RTCRST#	Ensure 10 ms–20 ms RC delay (8.2 K and 2.2 µF) See Figure 81

3. Changed: Processor Pin Names, Section 5.4, PGA370 Socket Definition Details, Table 12, Processor Pin Definition Comparison

Reference Section 5.4, PGA370 Socket Definition Details, Table 12, Processor Pin Definition Comparison:

Pin# AF36: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “DETECT”

Pin# AJ3: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “RESET” to “RESET2#”

Pin# Y1: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “RESERVED”

Pin# Z36: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “RESERVED”

4. Changed: Processor Pin Names, Section 4.1, Universal Motherboard Definition Details, Table 1, Processor Considerations for Universal Motherboard Design

Reference Section 4.1, *Universal Motherboard Definition Details*, Table 1, *Processor Considerations for Universal Motherboard Design*:

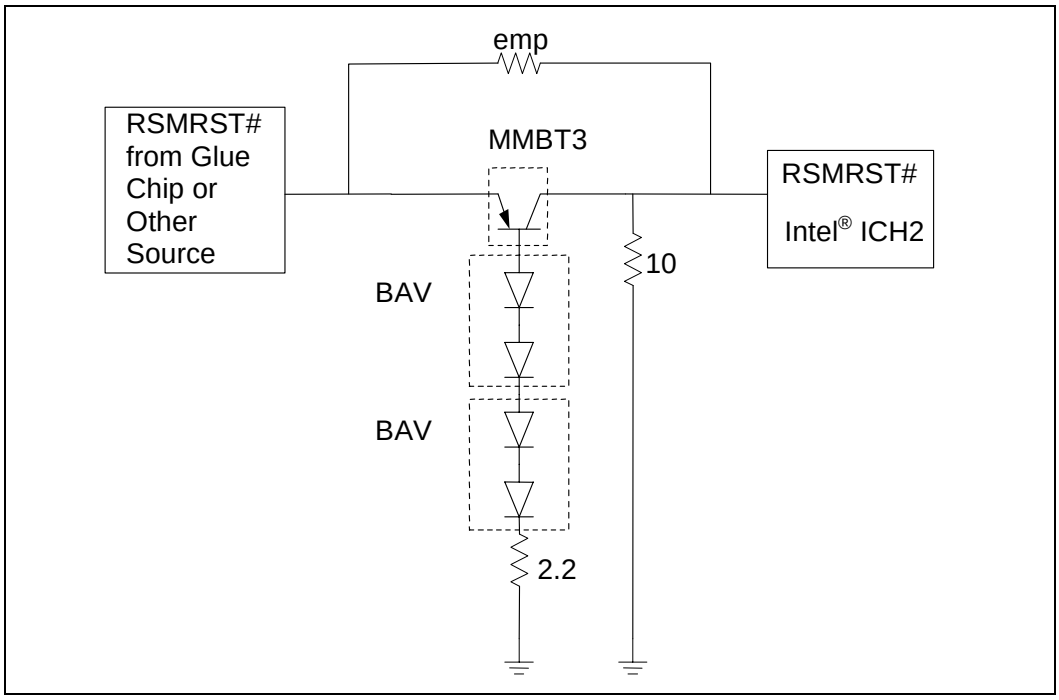
Pin# AF36: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “DETECT”

Pin# AJ3: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “RESET” to “RESET2#”

5. Changed: Added Information and Figure to Section 11.8.6, Power-Well Isolation Control Strap Requirements

Add the following information and figure to Section 11.8.6, *Power-Well Isolation Control Strap Requirements*:

The circuit shown in the figure below should be implemented to control well isolation between the 3.3 V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).



6. Changed: Section 14.4.9, *Power Management*; Modified

Change the Recommendations for RSMRST# in Section 14.4.9, *Power Management*, to read as shown below:

> "Connect to power monitoring logic, and should go high no sooner than 10 ms after both VccSUS3_3 and VccSus1_8 have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control as directed in Section 11.8.6."

7. Changed: Section 1.3.2.1, *Intel® 82815 GMCH Features*, Packaging/Power; Bullet Modified

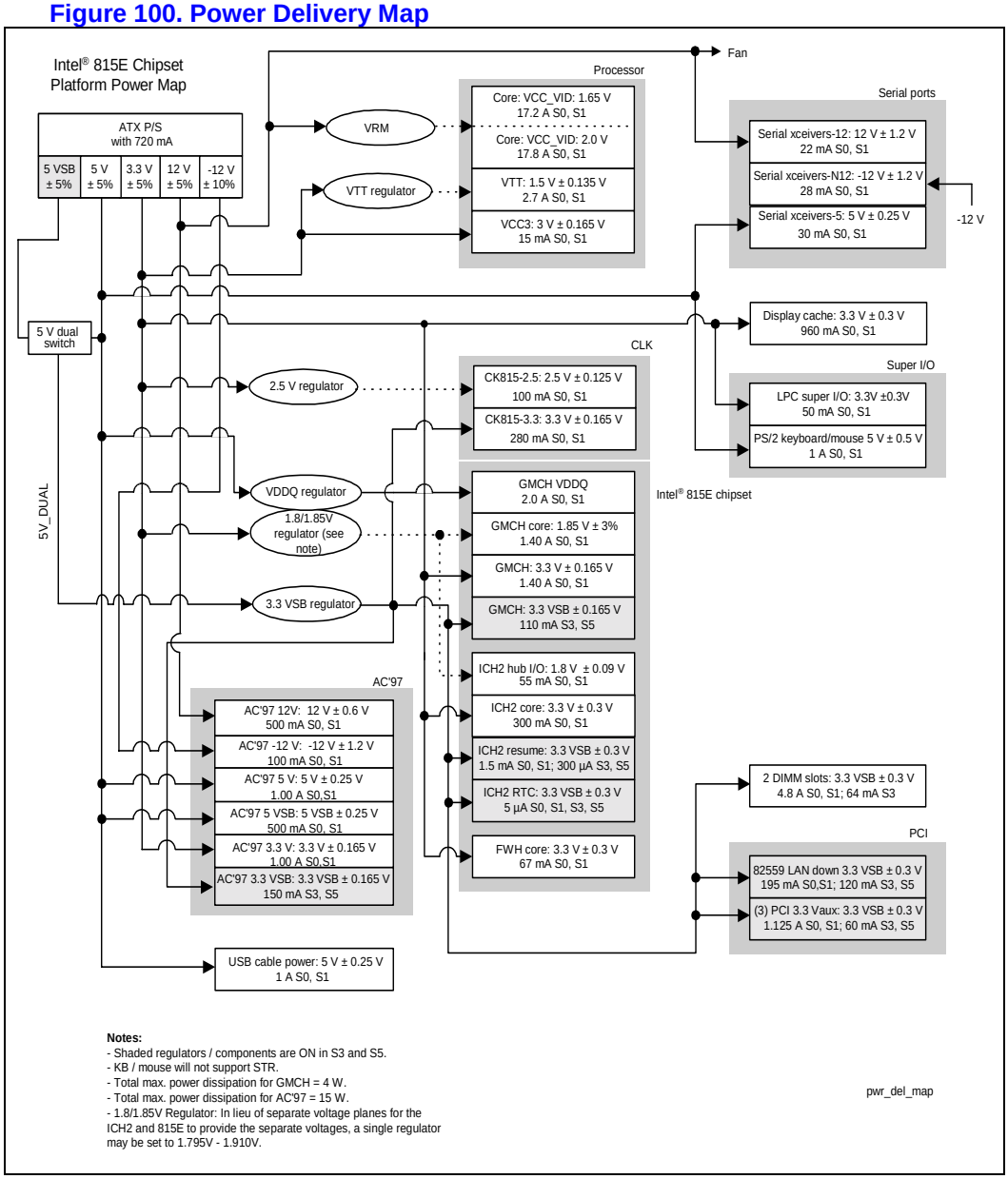
Reference Section 1.3.2.1, *Intel® 82815 GMCH Features, Packaging/Power*. Add the following information to the bullet so that it reads:

- 1.85 V core and mixed 3.3 V, 1.5 V, and AGTL+ IO. Note that the 82801BA ICH2 has a 1.8 V requirement and the 82815 GMCH has a 1.85V requirement. Instead of separate voltage regulators to meet these requirements, a single voltage regulator can be set to 1.795 V to 1.910 V. See Figure 100, *Power Delivery Map*.

8. Changed: Figure 100, *Power Delivery Map*; Replaced

See the following page.

Figure 100. Power Delivery Map



9. Added: Section 10.5 *Power_Supply PS_ON Considerations*

The following new section is added:

10.5 Power_Supply PS_ON Considerations

– If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to

be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

–The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

–The platform designer must ensure that the power supply used with the platform is not affected by this issue.

10. Changed: Section 14.4.12, *RTC*, Add SUSCLK to the Checklist

Add the following as a new checklist item to Section 14.4.12, *RTC*:

SUSCLK	• To assist in RTC circuit debug, route SUSCLK to a test point if it is unused.

11. Changed: Section 14.4.15, *Power, Modify Checklist Recommendations for 5V_REF_SUS*

Change the second bullet in the Recommendations column of the 5V_REF_SUS to the following:

V5REF_SUS affects 5V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5.

12. Changed: Section 13.3.3, *3.3V/V5REF Sequencing*

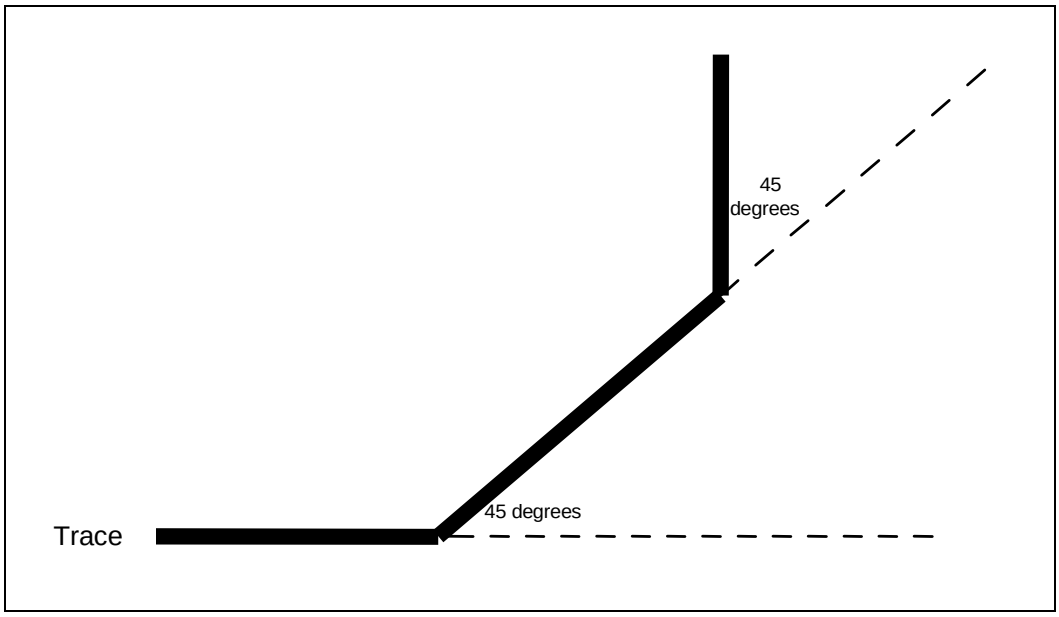
Change the second and third paragraphs of Section 13.3.3, *3.3V/V5REF Sequencing*, to the following:

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

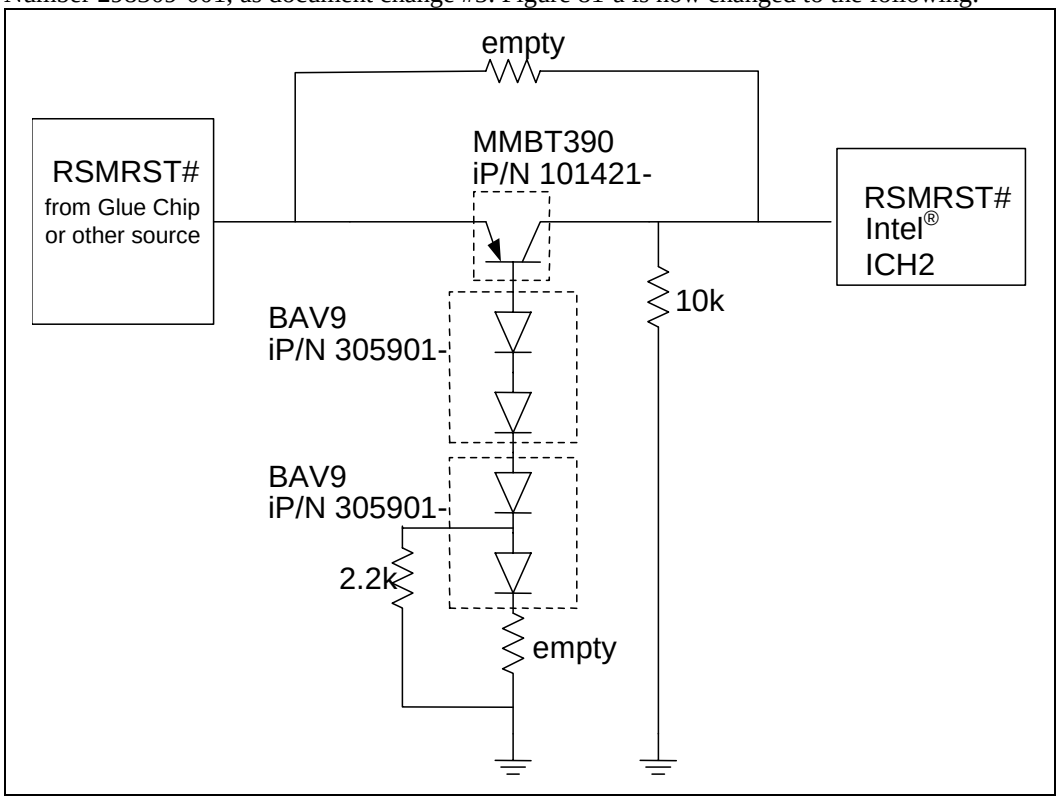
13. Changed: Figure 86, *Trace Routing*, in Section 11.9.2.1, *General Trace Routing Considerations*

Figure 86, *Trace Routing*, in Section 11.9.2.1, *General Trace Routing Considerations*, is replaced with the following figure:



14. Changed Figure 81-a, *RTC Power Well Isolation Control*, in Section 11.8.6, *Power Well Isolation Control Strap Requirements*

Figure 81-a, *RTC Power Well Isolation Control*, was added in the *Intel® 815E Chipset Platform for Use with Universal Socket 370 Design Guide Update*, dated October 12 2001, Document Number 298309-001, as document change #5. Figure 81-a is now changed to the following:



15. Changed Table 39, *Intel® CK-815 (2-DIMM) Clocks*, in Section 12.1, *2-DIMM Clocking*

The frequency entry for the 9 SDRAM clocks in Table 39, *Intel® CK-815 (2-DIMM) Clocks*, in Section 12.1, *2-DIMM Clocking*, is changed to "100/133 MHz".

Also, the first bullet under Table 39 is changed to show "100/133 MHz".

16. Changed Table 40, *Intel® CK-815 (3-DIMM) Clocks*, in Section 12.2, *3-DIMM Clocking*

The frequency entry for the 9 SDRAM clocks in Table 40, *Intel® CK-815 (3-DIMM) Clocks*, in Section 12.2, *3-DIMM Clocking*, is changed to "100/133 MHz".

17. Changed Section 13.3.3, *3.3V/V5REF Sequencing*

The first paragraph in this section is changed to read:

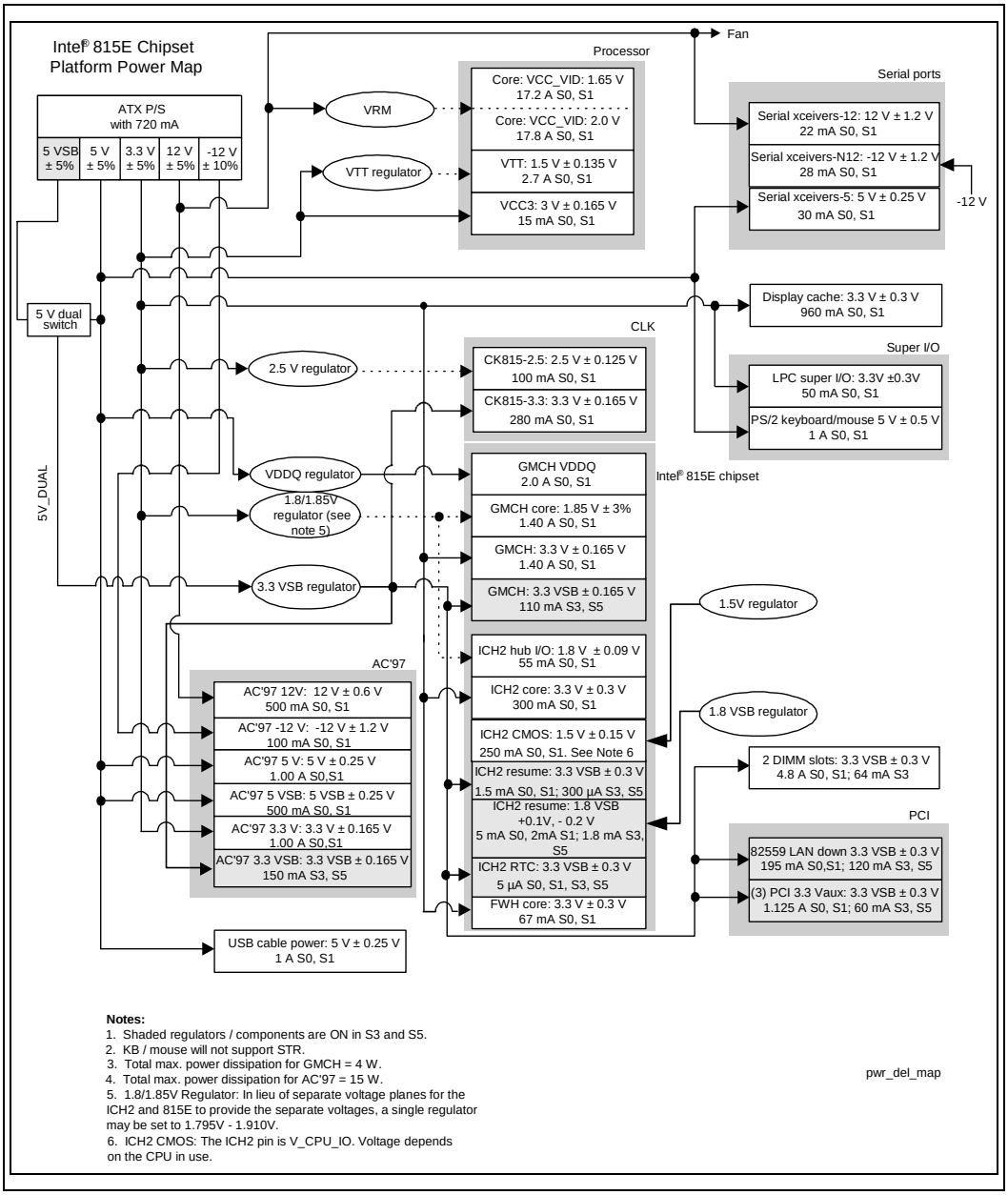
V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0 .7 V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 103 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

18. Changed Figure 100, *Power Delivery Map*, in Section 13*, Power Delivery*

Figure 100, *Power Delivery Map*, in Section 13, *Power Delivery*, was replaced by Document Change #8 in the public *Intel® 815E Chipset Platform Design Guide Update* 298594-005, dated March 2002. Figure 100 has two additional changes in the ICH2 section.

1. An ICH2 power plane is added to it. This added ICH2 power plane is "ICH2 CMOS". This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.
2. An ICH2 power plane is added to it. This added ICH2 power plane is "ICH2 Resume 1.8 VSB". This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.

Figure 100, *Power Delivery Map*, is replaced with the following:



19. Added Section 2.2, Electrostatic Discharge Platform Recommendations

The following new material is added as Section 2.2, *Electrostatic Discharge Platform Recommendations*:

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for

issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in Figures 1-4. In addition, a ground fill cutout should be placed on the Vcc layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as seen in Figure 2). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100-150 mils apart or less.

In conclusion, Intel recommends the following:

1. Fill the I/O area with the ground fill in all layers including signal layers whenever possible
2. Extend the ground fill along the entire back I/O area
3. Connect the ground fill to mounting holes
4. Place stitching vias 100-150 mils apart in the entire ground fill

Figure 1. Top Signal Layer before the Ground Fill near the I/O Layer

Figure 2. Top Signal Layer after the Ground Fill near the I/O Layer

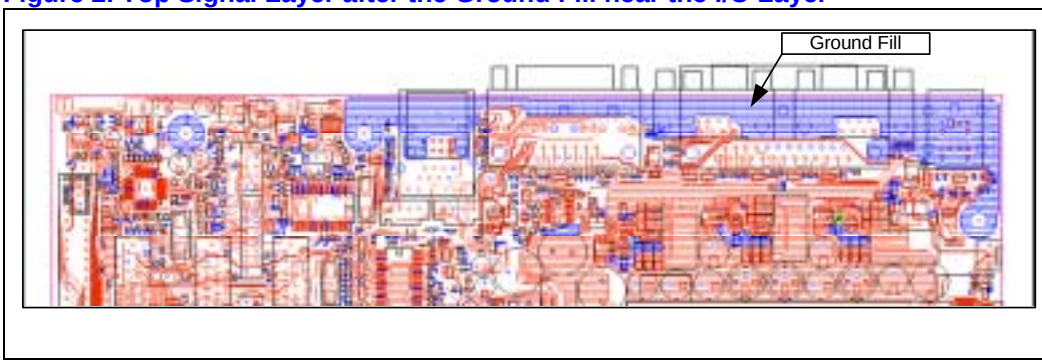


Figure 3. Bottom Signal Layer before fhe Ground Fill near the I/O Area

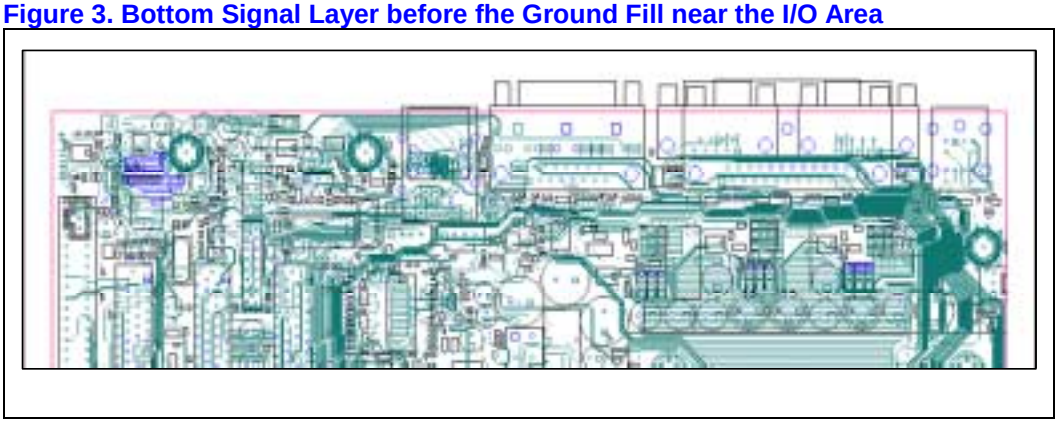


Figure 4. Bottom Signal Layer after the Ground Fill near the I/O