Intel® 82443ZX-M Design Guidelines

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Revision History

Rev.	Draft/Changes	Date
1.0	• Initial Release	May 1999

Reference Documents And Information Sources

Document Name or Information Source	Available From
Intel® 82443BX Data Sheet	www.intel.com
INTEL® 82440BX AGPset Design Guide	www.intel.com
82443BX Application Notes and Specification Updates	www.intel.com

Component Marking 82443ZX-M Host Bridge/Controller

Stepping	S-Spec	Top Marking	Freq.	Notes
A-0	SL3M5	FW8Z66M3BA	66MHz	Production

1. Overview

This information is being provided to Intel customers in order for them to begin developing a design with the Intel® 82443ZX-M. The 82443ZX-M is the basic mobile platform solution for the mobile Celeron™ processor.

The 82443ZX-M is a full featured 82443BX with the following exceptions:

- Maximum of 2 SO-DIMM sockets (256MB memory)
- No ECC
- Single processor support only (no support for IOAPIC)
- No Registered SO-DIMM support
- 66MHz-only host/DRAM bus frequency

2. Intel® 82443ZX-M Design Guidelines

The following design guidelines are provided in conjunction with the 82440BX Design Guides.

To support the 82443ZX-M, pin function has been changed as follows:

Ball Number	Previous Name	Previous Type of Pin	New Name	Relationship to Reduced Feature
AF24	CKE5/CSB7#	O	NC	1.0
AC23	CKE4/CSB6#	O	NC	1.0
AD23	CKE3/CSA7#	O	CKE3	1.0
AE24	CKE2/CSA6#	O	CKE2	1.0
AE16	CSA5#	O	NC	1.0
AD15	CSA4#	O	NC	1.0
AE25	CSB0#	O	NC	1.0
AD24	CSB1#	O	NC	1.0
AD26	CSB2#	O	NC	1.0
AC24	CSB3#	O	NC	1.0
AC26	CSB4#	O	NC	1.0
AB23	CSB5#	O	NC	1.0
AC12	WEB#	O	NC	1.0
AF17	MAA0	O	NC	1.0
AB16	MAA1	O	NC	1.0
AE17	MAA2	O	NC	1.0
AC17	MAA3	O	NC	1.0
AF18	MAA4	O	NC	1.0
AE19	MAA5	O	NC	1.0
AF19	MAA6	O	NC	1.0
AC18	MAA7	O	NC	1.0
AC19	MAA8	O	NC	1.0
AE20	MAA9	O	NC	1.0
AD20	MAA10	O	NC	1.0
AF21	MAA11	O	NC	1.0
AC21	MAA12	O	NC	1.0
AF25	MAA13	O	NC	1.0
AE13	DQMB1	O	NC	1.0
AD14	DQMB5	O	NC	1.0
AE11	MECC0	I/O	NC	2.0

Ball Number	Previous Name	Previous Type of Pin	New Name	Relationship to Reduced Feature
AA10	MECC1	I/O	NC	2.0
AA23	MECC2	I/O	NC	2.0
AA26	MECC3	I/O	NC	2.0
AF11	MECC4	I/O	NC	2.0
AD12	MECC5	I/O	NC	2.0
AA25	MECC6	I/O	NC	2.0
Y22	MECC7	I/O	NC	2.0

Note: All pins labeled NC are “No Connects” and should not be connected on the motherboard

Note: Relationship to Reduced Feature 1.0; Maximum of 2 SO-DIMM sockets (256MB memory)

Note: Relationship to Reduced Feature 2.0; No ECC

3. Intel® 82443ZX-M Register Changes

Register changes required to implement the 82443ZX-M device functionality are shown below. These specific register/bit combinations should be set as indicated below to support the 82443ZX-M. Refer to the Intel® 82440ZX AGPset: 82443ZX Host Bridge/Controller Data Sheet.

Register Name	Address Offset	Change To
NBXCFG - NBX Configuration Register (Device 0)	50-51h	Bit 31:24 - Note 1 Bit 17 - Note 2 Bit 15 - Note 3 Bit 8:7 - Note 4 Bit 6 - Not Applicable
DRAMC - DRAM Control Register (Device 0)	57h	Bit 4 - Not Applicable
DRB[0:7] - DRAM Row Boundary Registers (Device 0) 60h (DRB0) - 67h (DRB7)	64h-67h	Each should be programmed by the BIOS to the value established for address 63h, the DRB[3] value.
MBSC - Memory Buffer Strength Control Register (Device 0)	69-6Eh	Bit 31:28 - Not Applicable Bit 27:26 - Not Applicable Bit 23:22 - Not Applicable Bit 19:18 - Not Applicable Bit 9:6 - Not Applicable
RPS - SDRAM Row Page Size Register (Device 0)	74h-75h	Bit 15:8 - Not Applicable
SDRAMC - SDRAM Control Register (Device 0)	76h	Bit 4 - Not Applicable
ERRCMD - Error Command Register (Device 0)	90h	Bit 1 - Note 2 Bit 0 - Note 2
ERRSTS - Error Status Register (Device 0)	91h	Bit 7:0 - Not Applicable
MBFS - Memory Buffer Frequency Select Register	CA-CCh	Bit 18:16 - Not Applicable Bit 14 - Not Applicable Bit 12:11 - Not Applicable Bit 4:3 - Not Applicable

Note 1: These bits should all be set to “0” because the 82443ZX-M does not support ECC.

Note 2: This bit should be set to “0” because the 82443ZX-M does not support ECC.

Note 3: This bit should be set to “1” for single processor use. The 82443ZX-M does not support the I/O APIC or dual processors.

Note 4: These bits should be set to “00” because the 82443ZX-M does not support ECC.

4. Additional Information

1. All 82443BX Mobile Applications Notes, Design Guide Updates, and Specification Updates apply to the 82443ZX-M device. These documents are available http:\\www.intel.com.

2. Due to the design changes required to create the 82443ZX-M, complete NAND tree testing of this device is not possible.

3. New motherboard designs using the 82443ZX-M should have the MECCx pins disconnected at the SO-DIMM socket. If the “no-connect” associated with the MECCx pins is done at the 82443ZX-M socket, it is possible (when using 72-pin (ECC capable) memory modules) for the unterminated DQ pins carrying the ECC data to add noise to adjacent traces on the motherboard. Another option to prevent noise coupling from unused ECC pins is to limit SO-DIMM use to 64-pin (non-ECC) memory modules on motherboards using the 82443ZX-M.

4. The 82443ZX-M is available as a 66MHz-only host/DRAM bus device. The 82443ZX-M 66MHz-only device is S-Spec SL3M5 and QDF number Q823.

5. No board-level ICT test technique can be used to determine which device (82443BX or 82443ZX-M) is in the board.

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