



Intel® E7501 Chipset for Embedded Computing

Product Overview

The Intel® E7501 chipset represents the next step in high-performance chipset technology, supporting single- and dual-processor platforms optimized for the Intel® Xeon™ processor and Low Voltage Intel® Xeon™ processor. It also supports uni-processor platforms optimized for the Intel® Pentium® M processor. The design delivers maximized system bus, memory, and I/O bandwidth to enhance performance, scalability, and end-user productivity while providing a smooth transition to next-generation technologies.



Features that Maximize Performance of an Intel® E7501 Chipset-based Platform

- Dual Intel Xeon processors and a 400/533 MHz system bus provide up to 4.3 GB/s of available bandwidth
- Intel Pentium M processors and a 400 MHz system bus provide up to 3.2 GB/s of available bandwidth
- Single or dual DDR266 memory channels provide up to 4.3 GB/s of memory bandwidth
- Three hub interface 2.0 connections provide multiple high-bandwidth I/O configuration options, yielding up to 3.2 GB/s of I/O bandwidth

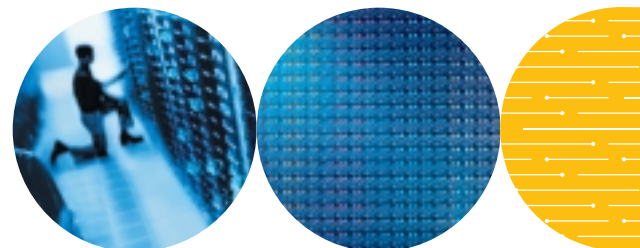
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Features

Benefits

Supports one or two Intel® Xeon™ processors or Low Voltage Intel® Xeon™ processors	■ Intel® NetBurst™ microarchitecture and the Hyper-Threading Technology of the Intel Xeon processor combine to deliver world-class performance.
Supports one Intel® Pentium® M processor	■ New microarchitecture supports low power and high performance.
400/533 MHz system bus capability	■ Up to 4.3 GB/s system bus bandwidth for increased memory and I/O throughput.
Intel hub architecture 2.0 connection to the Memory Controller Hub (MCH)	■ Point-to-point connection between the MCH and up to three P64H2 hub devices provides up to 3.2 GB/s of bandwidth. Error Correction Code (ECC) protection, coupled with high data transfer rates, supports I/O segments with greater reliability and faster access to high-speed networks.
PCI/PCI-X 64-bit controller hub	■ Next-generation PCI/PCI-X performance and significantly enhanced platform flexibility. Two independent 64-bit, 133 MHz PCI-X segments and two hot-plug controllers (one per segment) for each P64H2 hub allow up to six PCI-X buses per system.
Single/dual-channel DDR266 memory interface	■ Maximum memory bandwidth of 4.3 GB/s through a 144-bit wide, 266 MHz Double Data Rate SDRAM memory interface with densities up to 512 megabits.
Advanced Platform Reliability, Availability, Serviceability, Useability and Management (RASUM)	■ Memory ECC with Intel x4 Single Device Data Correction*, hardware memory scrubbing, MCH SMBus target interface, hub interface ECC, and the availability of enhanced error status information deliver increased platform reliability.

*In a x4 DDR memory device, the Intel x4 Single Device Data Correction (x4 SDDC), provides error detection and correction for 1, 2, 3, or 4 data bits within that single device and provides error detection, up to 8 data bits, within two devices in a dual-channel configuration. Single-channel provides error detection and correction for one data bit and provides error detection, up to two bits, within two devices.



Benefits of Advanced Technology and I/O Flexibility

The Intel E7501 chipset features modular design. It offers platform implementation flexibility to meet the expanding needs of uni- and dual-processor embedded computing applications, utilizing three core components:

- The Intel E7501 MCH is the central hub for all data passing through core system elements. This includes the Intel Xeon processors, via the system bus interface, the memory, via memory interface, and both the PCI/PCI-X 64-bit and I/O controller hubs, via Intel hub interfaces. The Intel E7501 chipset delivers compelling performance up to 4.3 GB/s of bandwidth across the 400/533 MHz system bus and up to 4.3 GB/s of bandwidth across two high-performance DDR memory channels, or up to 2.2 GB/s bandwidth across one DDR memory channel. The MCH also allows several high-bandwidth I/O configuration options for up to 3.2 GB/s of I/O bandwidth. Together, these features deliver high-throughput system performance.
- The Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) connects to the MCH through a point-to-point hub interface 2.0 connection. Up to three P64H2 devices can be attached to the MCH, each designed to provide an I/O bandwidth over 1.066 GB/s, for up to 3.2 GB/s of I/O bandwidth. Each P64H2 hub contains two independent 64-bit PCI-X interfaces and two PCI hot plug controllers, one per PCI-X interface. Each 64-bit PCI-X segment supports multiple PCI-X slots for high-bandwidth connectivity of next-generation components such as Intel® Gigabit Ethernet adapters and Intel® I/O processors.
- The Intel® 82801CA I/O Controller Hub 3 (ICH3-S) connects to the MCH through a point-to-point hub interface 1.5 connection. The ICH3-S provides legacy I/O interfaces through integrated features including a two-channel Ultra ATA/100 bus master IDE controller and three USB controllers for up to six USB 1.0 ports. The ICH3-S also offers an integrated System Manageability Bus 2.0 (SMBus 2.0) controller, an integrated LAN controller, and interfaces designed to meet AC'97 2.2 and PCI 2.2 standards.

Products	Package
The Intel® E7501 Memory Controller Hub (MCH)	1005 Flip Chip-Ball Grid Array (FC-BGA)
The Intel® 82801CA I/O Controller Hub 3 (ICH3-S)	421 Ball Grid Array (BGA)
The Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2)	567 Flip Chip-Ball Grid Array (FC-BGA)

Intel Access

Developer's Site:	developer.intel.com
Embedded Intel Architecture:	developer.intel.com/design/intarch
Intel® Technical Documentation Center:	appzone.intel.com/literature/index.asp (800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
General Information Hotline:	(800) 628-8686 or (916) 356-3104 5 a.m. to 5 p.m. PST

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