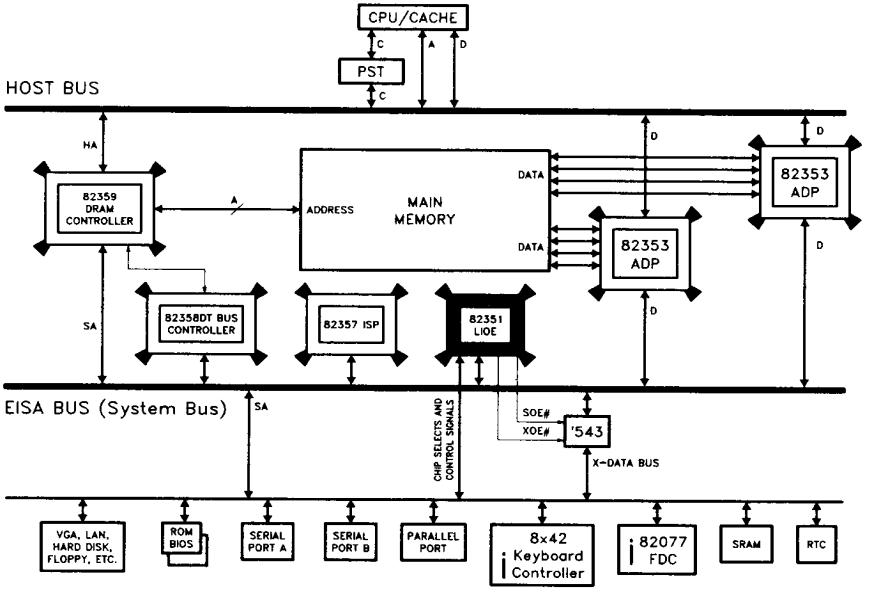
82351 LOCAL I/O EISA SUPPORT PERIPHERAL (LIO.E)

- **EISA and PC/AT System Fully Compatible Local I/O Controller**
- **Integrates:**
  - **— Local I/O Address Decoder**
  - **— EISA System Configuration Registers**
  - **— Fast CPU Reset and A20 Gate Port (92h)**
  - **— Two External Serial I/O Controller Interfaces with Four Assignable Interrupts Generation**
  - **— External Real Time Clock Interface**
  - **— External EISA Configuration RAM Interface**
  - **— Parallel Port Interface**
  - **— i486 and 386 CPU Compatible Numeric Co-Processor Interface**
  - **— External Floppy Disk Controller Interface**
  - **— External Keyboard (8x42) Controller Interface including Interrupt Generation**
  - **— EISA System ID Register**
- **Fast A20GATE, CPU RESET, and FLUSH# Generation by Snooping Keyboard Controller Commands**
- **Four Programmable General Purpose Chip Selects for Additional Local I/O Devices**
- **Provides I/O Address Decode and Commands**
- **Provides I/O Data Bus Buffer Control**
- **EPROM or FLASH EPROM BIOS ROM Interface (BIOS ROM Address is Externally Decoded)**
- **Edge or Level Sensitive Triggered Interrupt Generation Selection**
- **132 Pin PQFP Package**

  (See Packaging Specification Order Number 240800, Package Type KD)

Standard Configuration



290386-1

Figure 1-1. System Block Diagram

October 1992
Order Number: 290386-005

82351 LOCAL I/O EISA SUPPORT PERIPHERAL (LIO.E)

CONTENTS

CONTENTS

1

CONTENTS

CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

1.0 INTRODUCTION

The 82351 Local I/O EISA support peripheral (LIO.E) supports or integrates all of the I/O peripheral functions for a typical EISA system board with a minimum of external logic. This is illustrated by Figure 1-1 System Block Diagram. The LIO.E contains System Configuration, Status/Control Registers, Interrupt Logic, two Serial Port/Modem interfaces, one Real Time Clock interface, Parallel Port interface, local I/O bus address decoder, and data buffer control. The LIO.E can also be easily used in Non-EISA systems. The diagram in Figure 1-2 illustrates all the functions included in the LIO.E.

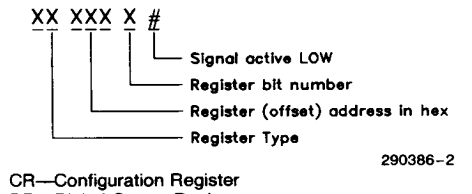
1.1 System Architecture Overview

The 82351 Local I/O EISA support peripheral (LIO.E) is located on the 8-bit peripheral bus. The peripheral bus is a buffered version of the 8-bit ISA bus which supports all of the motherboard I/O functions. The LIO.E provides the buffer control for each peripheral device located on this bus.

1.1.1 TYPES OF CYCLES SUPPORTED

- I/O Read
- I/O Write
- Memory Read from BIOS
- Memory Write to FLASH BIOS
- DMA Read from the Floppy Disk Controller
- DMA Write to the Floppy Disk Controller

1.1.2 REGISTER CODE USED IN DATASHEET



CR—Configuration Register
DR—Digital Output Register

Example: DR3x22—Digital Output Register 372 or 3F2 bit 2.

1.2 LIO.E Internal Architecture Overview

The major internal function blocks in the LIO.E are discussed in the following sections and are shown in Figure 1-2.

1.2.1 ADDRESS DECODER

The address decoder monitors the 16-bit system address SA(15:0) for all decodes. All I/O device address decodes are qualified with AEN# and REFRESH# inactive. The LIO.E Port Address I/O decode map is shown in Table 1-1.

To be compatible with the PC/AT architecture, alias address decoding is used. All of the port addresses provide X-Data bus buffer control (SOE#, XOE#), except port 00F0h.

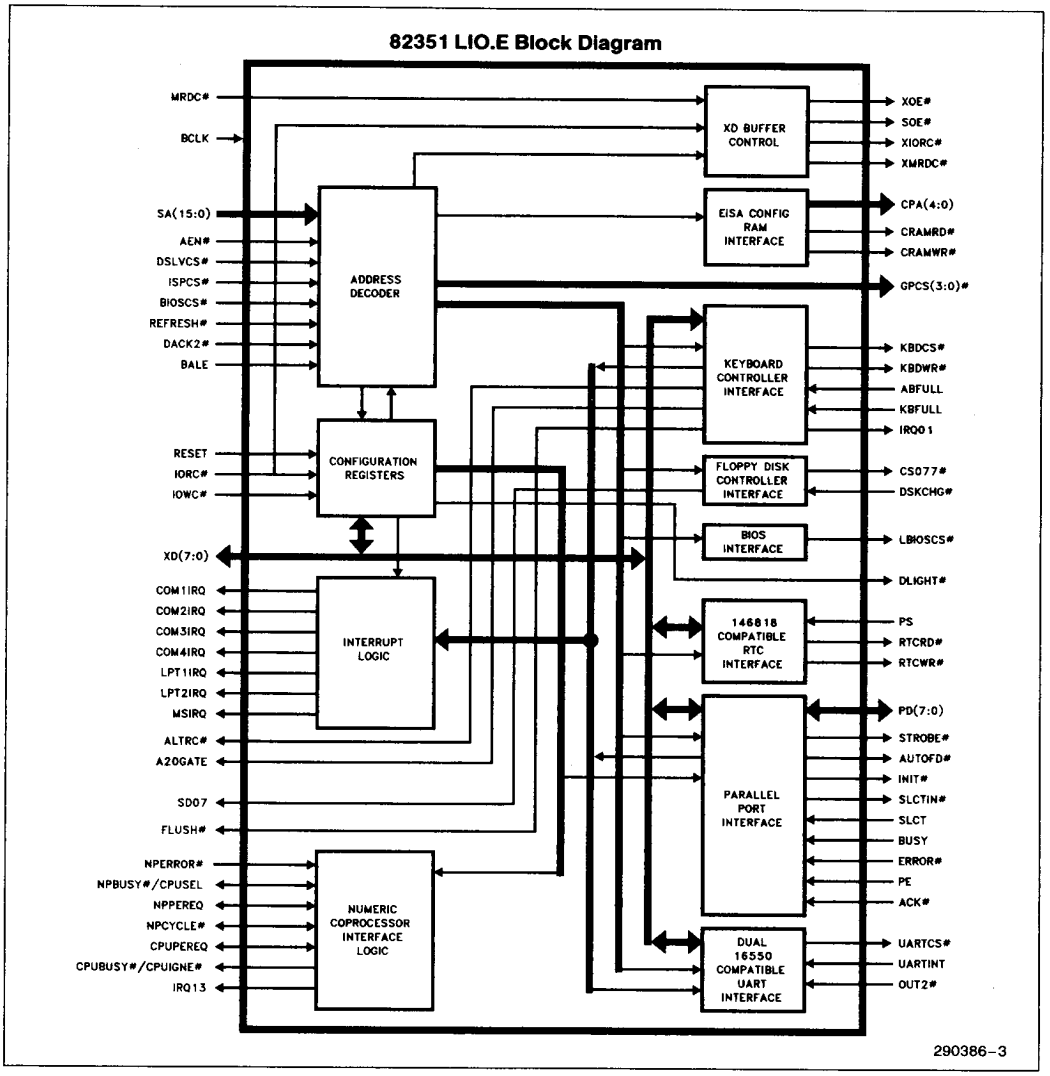


Figure 1-2. Internal Functional Block Diagram

Table 1-1. I/O Address Decode Map

Port	Address Bits				LIO.E Internal Register	Type	Signal Decode	Device
	FEDC	BA98	7654	3210				
0022h	0000	0000	0010	0010	Configuration	w	—	LIO.E
0023h	0000	0000	0010	0011	Configuration	r/w	—	LIO.E
0060h	0000	0000	0110	00x0	—	r/w	KBDCS#	LIO.E
0064h	0000	0000	0110	01x0	—	r/w	KBDCS#	LIO.E
0070h	0000	0000	0111	0xx0	—	w	RTCRD#/ RTCWR#	RTC Control —
0071h	0000	0000	0111	0xx1	—	r/w	RTCRD#/ RTCWR#	RTC Control —
0092h	0000	0000	1001	0010	System Control Port	r/w	—	LIO.E
00F0h	0000	0000	1111	0000	—	w only	IRQ13#	ISP
0278h	0000	0010	0111	1x00	Data Latch	r/w	—	Parallel Port (LPT3)
0279h	0000	0010	0111	1x01	Printer Status	r	—	Parallel Port (LPT3)
027Ah	0000	0010	0111	1x10	Printer Control	r/w	—	Parallel Port (LPT3)
027Bh	0000	0010	0111	1x11	—	r/w	—	—
027Ch	0000	0010	0111	1x00	Data Latch	r/w	—	Parallel Port (LPT3)
027Dh	0000	0010	0111	1x01	Printer Status	r	—	Parallel Port (LPT3)
027Eh	0000	0010	0111	1x10	Printer Control	r/w	—	Parallel Port (LPT3)
027Fh	0000	0010	0111	1x11	—	r/w	—	Parallel Port (LPT3)
02F8h	0000	0010	1111	1000	—	r/w	UARTCSB#	Serial Port (COM2)
02F9h	0000	0010	1111	1001	—	r/w	UARTCSB#	Serial Port (COM2)
02FAh	0000	0010	1111	1010	—	r	UARTCSB#	Serial Port (COM2)
02FBh	0000	0010	1111	1011	—	r/w	UARTCSB#	Serial Port (COM2)
02FCh	0000	0010	1111	1100	—	r/w	UARTCSB#	Serial Port (COM2)
02FDh	0000	0010	1111	1101	—	r	UARTCSB#	Serial Port (COM2)
02FEh	0000	0010	1111	1110	—	r	UARTCSB#	Serial Port (COM2)
02FFh	0000	0010	1111	1111	—	r/w	UARTCSB#	Serial Port (COM2)
0370h	0000	0011	0111	0000	Extended Mode	r/w	CS077#	Secondary FDC
0371h	0000	0011	0111	0001	Extended Mode	r/w	CS077#	Secondary FDC
0372h	0000	0011	0111	0010	Digital Output	w	CS077#	Secondary FDC
0373h	0000	0011	0111	0011	—	r/w	CS077#	Secondary FDC
0374h	0000	0011	0111	0100	—	r/w	CS077#	Secondary FDC
0375h	0000	0011	0111	0101	—	r/w	CS077#	Secondary FDC
0377h	0000	0011	0111	0x11	—	r/w	CS077#, SD07(r)	Secondary FDC, DSKCHG# Generation
0378h	0000	0011	0111	1x00	Data Latch	r/w	—	Parallel Port (LPT2)
0379h	0000	0011	0111	1x01	Printer Status	r	—	Parallel Port (LPT2)
037Ah	0000	0011	0111	1x10	Printer Control	r/w	—	Parallel Port (LPT2)
037Bh	0000	0011	0111	1x11	—	r/w	—	—
037Ch	0000	0011	0111	1x00	Data Latch	r/w	—	Parallel Port (LPT2)
037Dh	0000	0011	0111	1x01	Printer Status	r	—	Parallel Port (LPT2)
037Eh	0000	0011	0111	1x10	Printer Control	r/w	—	Parallel Port (LPT2)
037Fh	0000	0011	0111	1x11	—	r/w	—	—

Table 1-1. I/O Address Decode Map (Continued)

Port	Address Bits				LIO.E Internal Register	Type	Signal Decode	Device
	FEDC	BA98	7654	3210				
03BCh	0000	0011	1011	1100	Data Latch	r/w	—	Parallel Port (LPT1)
03BDh	0000	0011	1011	1101	Printer Status	r	—	Parallel Port (LPT1)
03BEh	0000	0011	1011	1110	Printer Control	r/w	—	Parallel Port (LPT1)
03BFh	0000	0011	1011	1111	—	r/w	—	Parallel Port (LPT1)
03F0h	0000	0011	1111	0000	Extended Mode	r/w	CS077#	Primary FDC
03F1h	0000	0011	1111	0001	Extended Mode	r/w	CS077#	Primary FDC
03F2h	0000	0011	1111	0010	Digital Output	w	CS077#	Primary FDC
03F3h	0000	0011	1111	0011	—	r/w	CS077#	Primary FDC
03F4h	0000	0011	1111	0100	—	r/w	CS077#	Primary FDC
03F5h	0000	0011	1111	0101	—	r/w	CS077#	Primary FDC
03F7h	0000	0011	1111	0x11	—	r/w	CS077#,	Primary FDC,
—	—	—	—	—	—		SD07(r)	DSKCHG# Generation
03F8h	0000	0011	1111	1000	—	r/w	UARTCSA#	Serial Port (COM1)
03F9h	0000	0011	1111	1001	—	r/w	UARTCSA#	Serial Port (COM1)
03FAh	0000	0011	1111	1010	—	r/w	UARTCSA#	Serial Port (COM1)
03FBh	0000	0011	1111	1011	—	r/w	UARTCSA#	Serial Port (COM1)
03FCh	0000	0011	1111	1100	—	r/w	UARTCSA#	Serial Port (COM1)
03FDh	0000	0011	1111	1101	—	r/w	UARTCSA#	Serial Port (COM1)
03FEh	0000	0011	1111	1110	—	r/w	UARTCSA#	Serial Port (COM1)
03FFh	0000	0011	1111	1111	—	r/w	UARTCSA#	Serial Port (COM1)
0800h–	0000	1000	xxxx	xxxx	EISA Config.	r/w	CRAMRD#/	RAM
08FFh	—	—	—	—	RAM Command		CRAMWR#	—
0C00h	0000	1100	0000	0000	EISA Config.	r/w	—	RAM
—	—	—	—	—	RAM Page	—	—	—
0C80h	0000	1100	1000	0000	EISA ID	r	—	LIO.E
0C81h	0000	1100	1000	0001	EISA ID	r	—	LIO.E
0C82h	0000	1100	1000	0010	EISA ID	r	—	LIO.E
0C83h	0000	1100	1000	0011	EISA ID	r	—	LIO.E
xxxxh	xxxx	xxxx	xxxx	xxxx	—	r/w*	GPCS(3:0)#	X-Bus Peripheral

NOTE:
*Accessible during all cycles: I/O, Memory, DMA, Refresh

1.2.1.1 Programmable General Purpose Chip Select Signals

There are four General Purpose Chip Select signals (GPCS(3:0)#) that can be used for any peripheral on the X-Bus. These chip select signals can be programmed through the Programmable Chip Select Low Order Address Registers (D4h–D7h) and High Order Address Registers (D8h–DBh). The system address is compared with the contents of these registers in order to generate any of these chip select signals. Each address bit comparison can be masked through the Programmable Chip Select Mask Register (D0h–D3h). The Peripheral Enable Register B (C1h) can be used to enable/disable any of these signals. More information can be found in the Configuration Register Section. Upon reset, each GPCSx# signal will remain inactive until both the Low and High Order Configuration Registers are programmed.

A programming example is shown below:

Program GPCS0# to AA55h

```
OUT 22h, D4h (IOWC# is active)
OUT 23h, 55h
OUT 22h, D8h
OUT 23h, AAh
```

1.2.2 CONFIGURATION REGISTERS

The configuration registers provide software flexibility to the LIO.E. They provide the enabling function for each supported peripheral device, interrupt selection, I/O device address select locations, EISA configuration RAM mapping, and various other features.

A complete description of the configuration registers can be found in the Register Description section.

1.2.3 BUFFER CONTROL LOGIC

The XD buffer logic provides control for an external 74F543 bi-directional transceiver to buffer the local peripheral data bus XD(7:0) from the system data bus SD(7:0). In order to prevent contention between XD(7:0) and SD(7:0) or between the 74F543 and local peripheral devices, the LIO.E generates XIORC# and XMRDC# which are delayed versions of IORC# and MRDC# respectively. Figure 1-3 below describes the behavior of these buffer control signals.

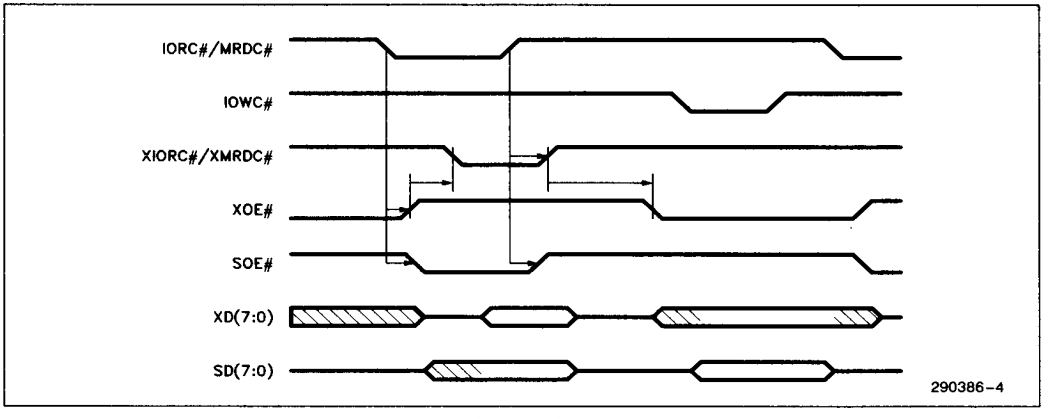


Figure 1-3. Buffer Control Signal Functionality

1.2.3.1 XOE# Generation

As shown in Figure 1-3, the active edge of XIORC# and XMRDC# are generated from the delayed version of the XOE# inactive edge, while the inactive edges are generated directly from IORC# and MRDC# inactive edges. This prevents the buffered peripheral from driving XD(7:0) until the 74F543 has had time to float its outputs. The active edge of XOE# is generated from the delayed inactive edge of XIORC# or XMRDC# to allow time for the peripheral device to float XD(7:0) from XIORC# or XMRDC# before re-driving XD(7:0). However, the re-drive time cannot be excessive since the following cycle could be a write cycle and could be re-driven as early as 120 ns from the inactive edge of IORC# or MRDC#. XD(7:0) will need to meet a positive setup to the following active IOWC# signal.

XOE# is normally active, except for the following conditions:

- I/O Read Cycles
- Memory Read Cycles
- I/O Write Cycles to the Floppy Disk Controller when CRC42 = 0

The default condition for XOE# is active if no cycles are occurring. Table 1-2 shows the generation of the X-Bus Command Signals.

1.2.3.2 SOE# Generation

SOE# is normally inactive except during:

1. LIO.E Resident Register I/O Read Access
2. External I/O Read to the EISA Configuration RAM
3. I/O Bus Resident Slave Read Access
   - Serial Port
   - Parallel Port
   - RTC
   - Keyboard
   - General Purpose Chip Selects GPCS(3:0)
   - FDC
4. DMA I/O Read Access to Floppy Disk
5. Non-DMA I/O Read Access to the ISP
6. Non-DMA Access to the DRAM Slave Port
7. Memory Read Access to ROM

SOE# will be disabled for an access to a peripheral that is not enabled via the LIO.E configuration registers.

1.2.3.3 X-Bus Commands

The X-Bus control signals XIORC# and XMRDC# are generated from IORC# and MRDC# respectively. They should be used by peripherals located on the X-Bus in order to avoid contention with the 74F543 buffer. The signals CRAMRD# and RTCRD# have similar timings. The default state of XIORC# and XMRDC# are inactive.

In order to provide enough write data hold time for write command signals generated by the LIO.E, these command signals (CRAMWR#, RTCWR#, and KBDWR#) are terminated after a maximum active time of 4 BCLKs (minimum of 3 BCLKs). Figure 1-4 illustrates the behavior of these signals.

Since all system bus cycles to LIO.E supported peripherals execute with a command width of 4.5 BCLKs, there is always at least ½ BCLK of write data hold time.

Table 1-2. X-Bus Command Signal Generation

Cycle	AEN#	REFRESH#	IORC#	MRDC#	BIOSCS#	XIORC#	XMRDC#	SOE#	XOE#
Default	x	1	1	1	x	1	1	1	0
I/O Read	1	1	0	1	x	0	1	0	1
Memory Read	1	1	1	0	1	1	0	1	0
Memory Read to BIOS ROM	1	1	1	0	0	1	0	0	1
DMA I/O Read	0	1	0	1	x	0	1	0	1
DMA Memory Read	0	1	1	0	x	1	1	1	0
REFRESH	x	0	x	x	x	1	1	1	0

NOTE:
SOE# active is assumed qualified by LIO.E I/O decode map and configuration register selection.

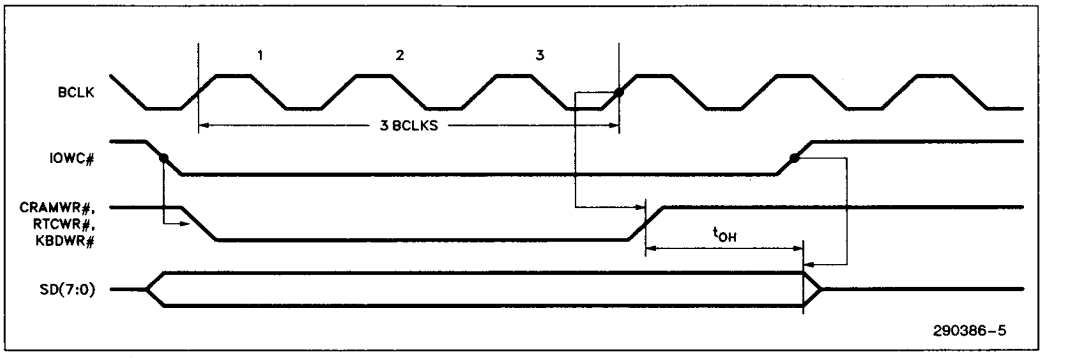


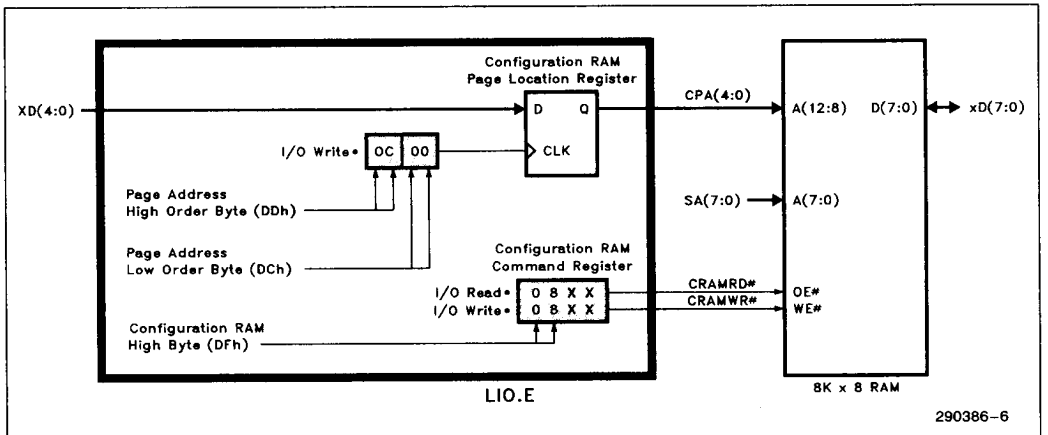
Figure 1-4. Write Command Signal Functionality

1.2.4 EISA CONFIGURATION RAM SUPPORT

The LIO.E provides the control signals for 8 Kbytes of external configuration RAM which is used for storing EISA system parameters. The configuration RAM is I/O mapped and organized in pages of 256 bytes. The Configuration RAM Interface diagram shows how the LIO.E internal configuration registers control the external RAM. The Configuration RAM I/O location is programmable using the internal Configuration RAM Page Location Registers A and B (DCh and DDh). During an I/O write to this programmed page location address, XD(4:0) is latched and driven as CPA(4:0) from the LIO.E for the RAM's upper byte address decode A(12:8).

The Configuration RAM Command Register (DFh) can be programmed to remap the high byte of the RAM I/O address location. The high byte of the address location programmed in the Configuration RAM Command Register is compared with the I/O address bits SA(15:8) to generate CRAMWR# or CRAMRD#. The RAM is enabled when either of these signals are generated. The low byte of the address is sent to the RAM via the SA address bus SA(7:0).

Caution: Programming the RAM Page Location and Command Register with the same data may cause errors while writing to the Configuration RAM.



NOTE:
Default Register Values are in shaded boxes.

Figure 1-5. Configuration RAM Interface

The programming examples that follow start with default values assumed.

Example 1: Write to page register using default value.

Using the Default Address Location for the Configuration RAM Page Registers and Command Register, Write Peripheral Device I.D. Value of 00h to Address Location 1F12h, and Read that Location's Data

	Address	Data	
OUT	0C00	1Fh	Load 1Fh into the Page Register to be latched as CPA(4:0).
OUT	0812h	00h	Store at address location 1F12h peripheral I.D. value 00h.
IN	0812h	data	12h is sent on the SA(7:0) bus to read from RAM location 1F12h. CRAMRD# and IORC# are active. Data is returned.

Example 2: Program the Configuration RAM Page Register Location (DCh and DDh) to 1213h and Program CPA(4:0) with 16h

	Address	Data	
OUT	22h	21h	Identify LIO.E for programming (access), IOWC# is active
OUT	23h	02h	
OUT	22h	DCh	Program page location registers
OUT	23h	13h	
OUT	22h	DDh	
OUT	23h	12h	
OUT	1213h	16h	Load 16h into Page Location Registers to be latched as CPA(4:0). IOWC# to 1213h generates the clock to the internal page register.

Read from RAM Location 16AAh

	Address	Data	
IN	08AAh	data	"AAh" points to the address in RAM (low order byte on the SA(7:0) bus), and data is read from that location. CRAMRD# and IORC# are active

Remap Configuration RAM Command Register to 27xxh

	Address	Data
OUT	22h	DFh
OUT	23h	27h

Read Address 1668h from RAM

	Address	Data	
IN	2768h	data	(16h is already latched in the Page Location Registers, 68h is sent on the SA(7:0) address bus in order to read RAM location 1668h. IORC# to 27xxh generates CRAMRD#. Data is read from that location.)

Example 3:

Map the Configuration RAM Page Location Register to 2815h, the Configuration RAM Command Regsiter to 01XXh, Read the RAM Location 1793h, and Write to the RAM Location 13ABh with 66h Data

	Address	Data	
OUT	22h	21h	Identify LIO.E for programming (access), IOWC# is active
OUT	23h	02h	
OUT	22h	DCh	Program page location registers
OUT	23h	15h	
OUT	22h	DDh	
OUT	23h	28h	
OUT	22h	DFh	Program command register
OUT	23h	01h	
OUT	2855h	17h	Load 17h into Page Location Register to be latched as CPA(4:0)
IN	0193h	data	(93h is sent on the SA(7:0) address bus to read RAM location 1793h. CRAMRD# and IORC# are active. Data is returned.)
OUT	2855h	13h	(load 13h into Page Location Register to be latched as CPA(4:0). IOWR# is active.
OUT	01ABh	66h	(66h is written to RAM location 13ABh. CRAMWR# and IOWR# are active.)

1.2.5 KEYBOARD CONTROLLER INTERFACE

The LIO.E provides the chip select and read/write commands for an external 8x42 keyboard controller. To support keyboard controllers that provide a mouse interface, the LIO.E generates the mouse interrupt (MSIRQ) from the 8x42 ABFULL signal.

In order to provide for faster switching of the 8x42 signals, ALTRC# (CPU reset) and A20GATE (address 20 enable), the LIO.E monitors the keyboard commands via XD(7:0) and generates these signals in behalf of the keyboard controller. If ALTRC# (from System Register 92h or by snooping keyboard commands), or A20GATE (from bit 1 of the System Register 92h or by snooping keyboard commands) is detected, KBDWR# will be prevented from going active with IOWC#. This effectively blocks the command to the keyboard controller, allowing it to be available for the next command much sooner.

1.2.5.1 Keyboard Chip Select

KBDCS# is generated whenever there is an I/O access to the 60h, 62h, 64h or 66h addresses and bit 2 of Peripheral Enable Register A (COh) is "1".

1.2.5.2 Keyboard Write Command Generation

The KBDWR# signal is generated whenever there is a write cycle to register 60h, 62h, 64h or 66h except for the following cases:

1. The KBDWR# signal (keyboard write) is prevented from going active during an I/O write cycle, if the keyboard command to generate ALTRC# is detected.
2. If an I/O write to register 64h with data contents FFh (null command) is detected immediately following case one above, the LIO.E will hold KBDWR# inactive.

It should be noted for the purposes of inhibiting KBDWR# that the data contents for I/O writes to 0060H are ignored except when the data of the preceding I/O write to 0064H is D1H.

1.2.5.3 ALTRC# Generation

The ALTRC# signal is generated by the following mechanisms:

The first two cases are enabled if bit 4 of Peripheral Enable Register B (C1h) is "1". Also, KBDWR# is blocked for the first two cases.

1. ALTRC# (Alternate CPU Reset) is generated whenever an I/O write is detected to Register 64h with FOh–FEh even data. ALTRC# is pulsed low for 3–4 BCLKs and is activated from the rising edge of IOWC# on BCLK's falling edge.
2. ALTRC# is generated whenever Register 60h is written after Register 64h is written with the data contents of D1h. Bit 0 of the 60h write is latched and driven out as ALTRC#.
3. ALTRC# is generated whenever System Control Register 92h Bit 0 = 0 and it is then written a "1". CRC15 is a "1" during this time. If 92h Bit 0 = "1" and a "1" is written, ALTRC# is not generated.

1.2.5.4 A20GATE Generation

A20GATE is generated by the following two mechanisms:

1. Whenever I/O Register 60h is written after 64h with data contents of D1h, the data bit XD1 is latched and is driven out as A20GATE. From the BCLK falling edge when IOWC# is driven active, this function is enabled only if bit 4 of Peripheral Enable Reg. B is equal to "1". KBDWR# is inhibited for this case.
2. Whenever System Control Port 92h is written, the data bit XD1 is latched and driven as A20GATE from the falling edge of BCLK when IOWC# is driven active. The 82351 will latch the last A20Gate value written from either of the above 2 methods.

1.2.5.5 FLUSH# Generation

FLUSH# (Cache Flush) is generated whenever A20GATE changes its state. FLUSH# is the active low pulse of nominally 2 to 3 BCLKs duration (similar to ALTRC#).

1.2.6 FLOPPY CONTROLLER INTERFACE

The LIO.E supports the 82077 floppy disk controller. A chip select is provided along with the buffering of the drive interface signal DSKCHG#. Since this signal is driven from a register location that is also shared by PC/AT compatible hard disk controllers, only the applicable data bus bit (SD07) is driven onto the system bus when this register location is selected (I/O read from 03F7h or 377h).

In order to provide for proper chip select setup, the CS077# signal is activated for the primary FDC addresses, 03F2h, 03F3h, 03F4h, 03F5h and 03F7h (or secondary addresses 0372h, 0373h, 0374h, 0375h, and 0377h) without regard to the I/O commands. However, the buffer enable function for SOE# is only active for I/O reads from 03F2h, 03F3h, 03F4h, and 03F5h (or 0372h, 0373h, 0374h, or 0375h).

Table 1-3. CS077# Generation

SA(0:15)	CRC03	CRC41	CRC40	DSKCHG#	CS077#
X	X	X	X	0	1
X	0	X	X	X	1
0370H	1	1	1	1	0
0370H	1	0	1	1	1
0371H	1	1	1	1	0
0371H	1	0	1	1	1
0372H–0377H	1	X	1	1	0
03F0H	1	1	0	1	0
03F0H	1	0	0	1	1
03F1H	1	1	0	1	0
03F1H	1	0	0	1	1
03F2H–03F7H	1	X	0	1	0

NOTE:
03F6h/0376h are not included in the 03F0–03F7h/0370–037Fh address range.

If the hard disk interface is located on the X-Data Bus (as indicated by CRC42 = 1), then SOE# will go active for an I/O read of 3F7h (or 377h) as well.

If the extended register mode is selected via the FDC configuration register, CS077# and SOE# will also go active for addresses 0370h, 0371h, 03F0h and 03F1h.

This block generates the chip select for the external 82077 Floppy Disk Controller and drives SD07 whenever Disk Change input is active during 03F7h I/O register access. The Buffer Control Logic controls the Buffer direction and output enable during FDC slave read/write and FDC DMA read/write. This Block is enabled if both of the following are true:

1. Bit 3 of CRC0 Register is "1".
2. DSKCHG# is sampled HIGH upon RESET falling edge.

1.2.6.1 FDC Chip Select (CS077#)

This signal is generated after decoding external address SA0–SA15, and bit 0 and 1 of the Configuration Register at offset address C4h. Table 1-3 shows CS077# Generation. More information about Register C4h is located in the Configuration Register Section.

1.2.6.2 SD07 Generation

Table 1-4 shows the Floppy Disk Controller Signal states.

Table 1-4. FDC Control Signal States
Floppy Control Signal States for an I/O read of 03F7h

CRC42	CS077#	SD07	SOE#	XD7
0	0	$\overline{\text{DSKCHG\#}}$	1	FLOAT
1	0	FLOAT	0	$\overline{\text{DSKCHG\#}}$

1.2.7 BIOS INTERFACE

The LIO.E supports the system board BIOS by providing the LBIOSCS# output. This signal is derived from the BIOSCS# input latched from the falling edge of BALE#. The address decode for the BIOS ROM is done externally and is provided to LIO.E as BIOSCS#. The Buffer control for BIOS ROM accesses by the CPU is handled by the XD Buffer Control Logic. Table 1-5 shows the conditions in which LBIOSC# is generated.

Table 1-5. LBIOSCS# Generation

MRDC#	AEN#	BIOSCS#	XMRDC#	LBIOSCS#
0	1	0	0	0
1	1	0	1	0
X	1	1	X	1
0	0	X	0	1

1.2.8 REAL-TIME CLOCK INTERFACE

The LIO.E contains external RTC support. It decodes the RTC I/O location and provides read/write strobes (RTCWR#, RTCRD#). See Figure 1-6 RTC Interface Block Diagram.

Password support via I/O register 92h is also supported. If bit 3 of register 92h is set to a "0" at powerup, the RTC can be accessed by RTCWR# and RTCRD# active and any register on the RTC can be accessed. If bit 3 of register 92h is set to a "1", accesses to 36h–3Fh are inhibited. Note that access is not inhibited on accesses to B6h–BFh which alias to 36h–3Fh. The address latch is a duplicate of the latch on the RTC.

If access is allowed and the Peripheral Enable Register A (C0h) bit 1 is a "1", then the RTC Address Register (70h, 72h, 74h, 76h) and Data Register (71h, 73h, 75h, 77h) can be used to read or write to the RTC.

A conceptual programming example follows:

1. Write 70h with the RTC Register Address
2. Read/Write 71h with the data

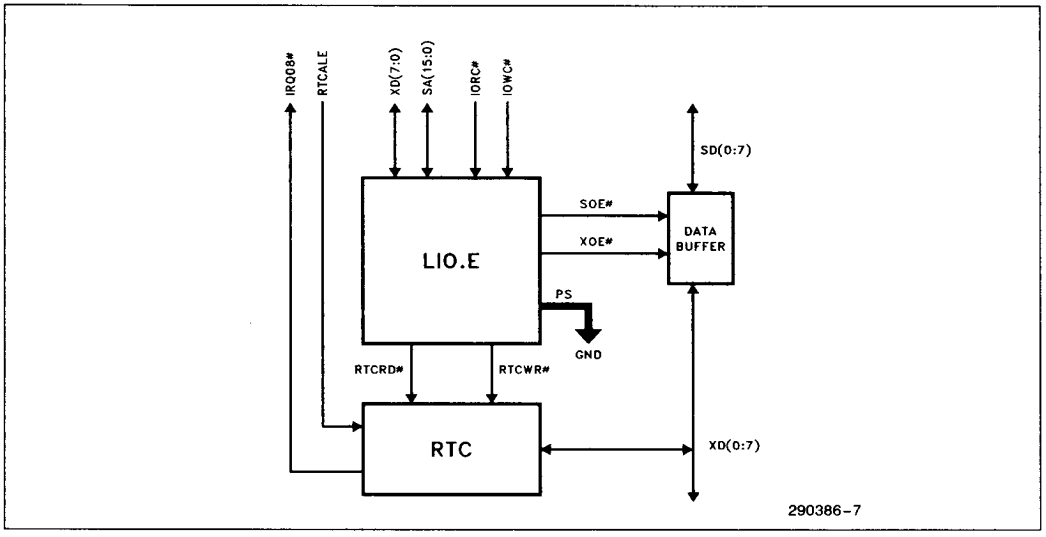


Figure 1-6. RTC Interface Block Diagram

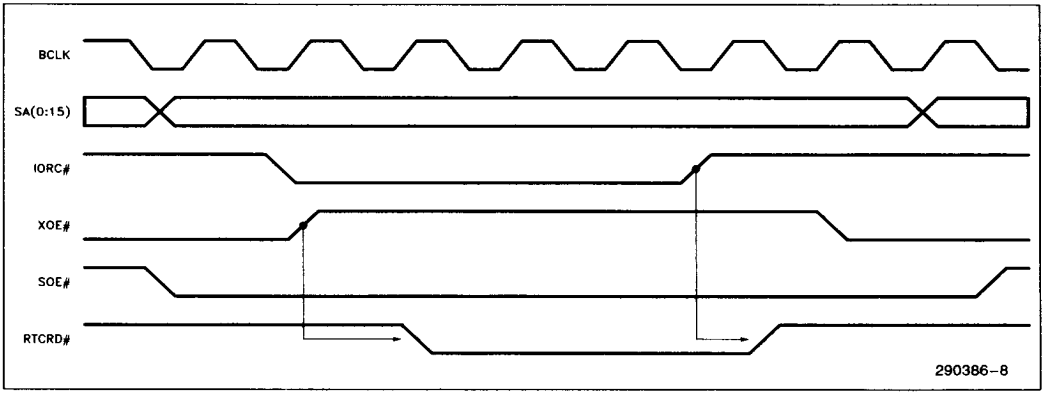


Figure 1-7. RTCRD# Generation

1.2.9 PARALLEL PORT INTERFACE

Register	LPT1	LPT2	LPT3
Data Latch (r/w)	03BCh	0378h/037Ch	0278h/027Ch
Printer Control (r/w)	03BEh	037Ah/037Eh	027Ah/027Eh
Printer Status (r)	03BDh	0379h/037Dh	0279h/027Dh

The LIO.E contains an implementation of a fully compatible PC/AT parallel port, which includes added functionality. The control signals are designed to attach directly to the parallel port system connector without additional external buffering. In addition, it contains the enhanced capability of bidirectionality (i.e., scanner support), and interrupts that can be configured for either edge or level compatibility. The Parallel Port Registers are listed above:

Each of these registers can be accessed through the LPT1, LPT2, or LPT3 assigned address selected by the Printer Configuration Register (C2h) bits 1 and 0. The Parallel Port Interface can also be disabled by the same bits. The Data Latch direction is programmable through the Printer Configuration Register (C2h) bit 2. Register descriptions are located in the configuration register section. To support bi-directional capability on the parallel port, bit 2 of the printer configuration register at the offset address of C2h allows the output data bus drivers PD(7:0) to be tri-state so that they can be used as inputs.

1.2.10 DUAL SERIAL CHANNEL INTERFACE

The LIO.E integrates all of the logic necessary for a direct connect to two serial UARTs (i.e., 16550A). See Figure 1-8 Serial I/O Interface. The address decode is provided by UARTCSA# and UARTCSB#. Each of these chip selects can be configured for the standardized address of COM1 or COM2, or a fully programmable address to support COM3 or COM4.

The interrupt signals from the external UARTs are connected to the LIO.E pins UARTINTA and UARTINTB. Each interrupt source can then be selected out on COM1IRQ, COM2IRQ, COM3IRQ, or COM4IRQ via configuration register (C5h). The interrupt outputs can also be configured as either edge or level compatible. See the Interrupt Control and Configuration Register sections for more information.

As in the PC/AT implementation, the active OUT2x# signal is used to enable the corresponding serial channel interrupt (COMxIRQ). Serial port assignments determine whether a port will be enabled or disabled. See Table 1-6 Serial Port Assignments. For example, if Serial Port A and Serial Port B are mapped to the same address location, only Serial Port A will be selected and COMxIRQ will be generated from UARTINTx.

Table 1-6. Serial Port Assignments

Assignments	Serial Port A		Serial Port B	
	UARTCSA#	COMxIRQ	UARTCSB#	COMxIRQ
COM1 and COM2 Mapped to Same Address, Different COMxIRQ	Enabled	Enabled	Disabled	Disabled
COM1 and COM2 Mapped to Different Address, Same COMxIRQ	Enabled	Enabled	Enabled	Enabled
COM1 and COM2 Mapped to Same Address, Same COMxIRQ	Enabled	Enabled	Disabled	Disabled
COM1 and COM2 Mapped to Different Address, Different COMxIRQ	Enabled	Enabled	Enabled	Enabled

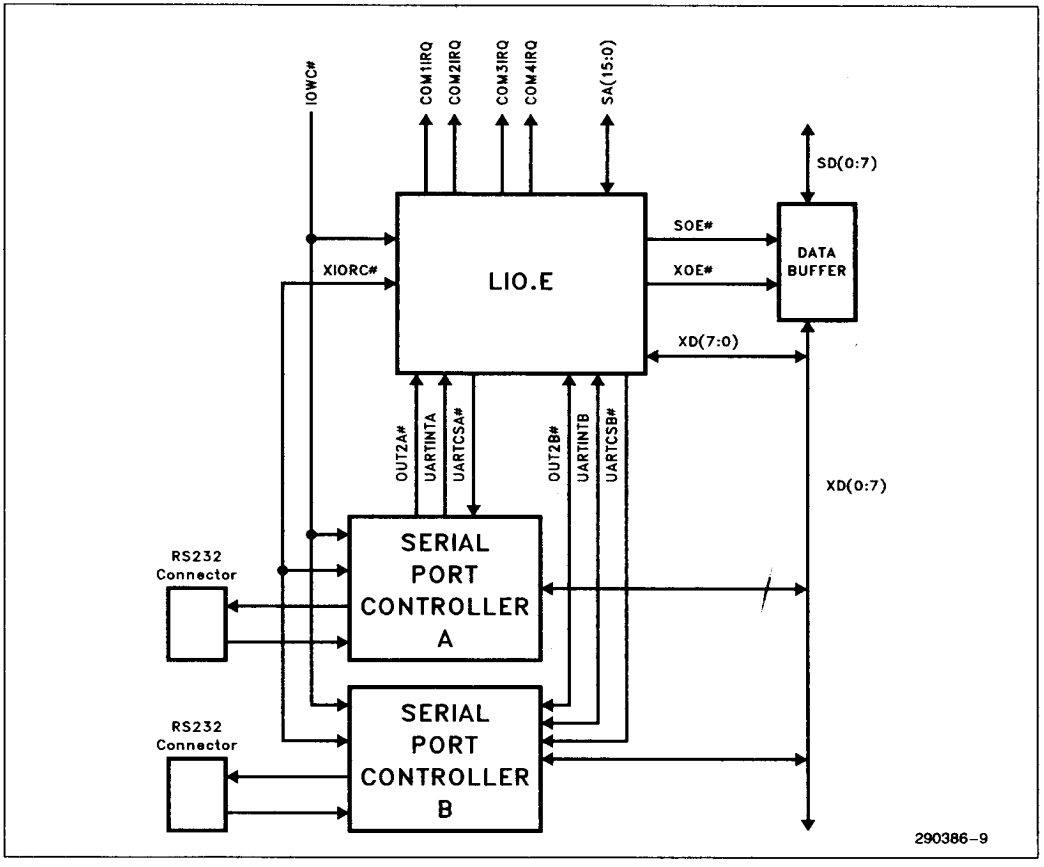


Figure 1-8. Serial I/O Interface

1.2.11 INTERRUPT CONTROL LOGIC

The interrupt control logic selects and enables the parallel port, serial channels, keyboard, and mouse interrupts by programming their respective configuration registers.

1.2.11.1 Keyboard Interrupt Generation

The keyboard interrupt to the 8259A core of the ISP (IRQ01) is an edge compatible interrupt only. It is generated from the rising edge of KBFULL from the 8x42 keyboard controller. IRQ01 is cleared by an I/O read from 0060h or by a reset.

1.2.11.2 Mouse Interrupt Generation

The mouse interrupt (MSIRQ) is enabled by the configuration register C1h. This interrupt can be configured for either edge or level compatibility. This signal is activated from the rising edge of ABFULL by the keyboard controller. It is deactivated by an I/O read from 0060h, or by a reset, or when configuration register C1h bit 6 is written as an "0". In the edge compatible mode it is active high, while in the level compatible mode it is open collector and can be shared by other open collector interrupt sources. Please refer to the configuration register section and pin description for complete detail.

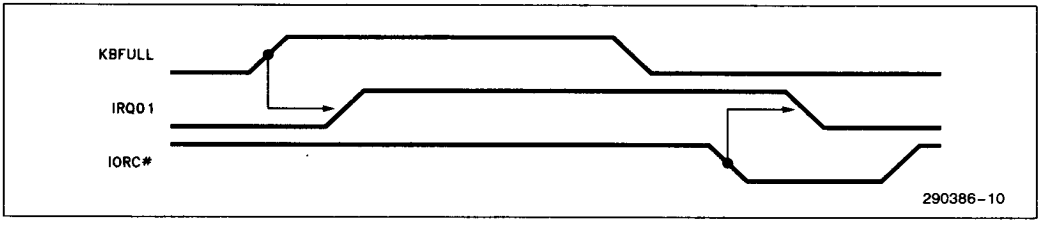


Figure 1-9. Keyboard Interrupt Generation

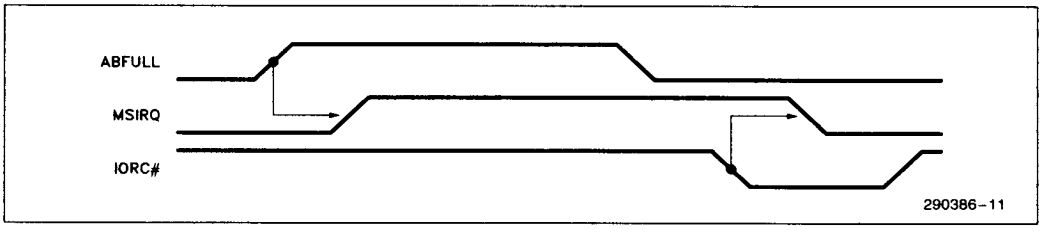


Figure 1-10. Mouse Interrupt Generation (Edge Compatible Mode)

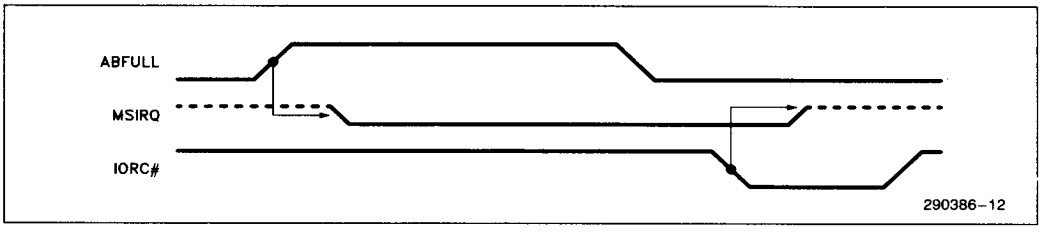


Figure 1-11. Mouse Interrupt Generation (Level Compatible Mode)

1.2.11.3 Parallel Port Interrupt Generation

The parallel port of the LIO.E can generate an interrupt on either LPT1IRQ or LPT2IRQ from the ACK# signal. The interrupt output can be configured as either edge or level compatible. The configuration register C2h controls the interrupt operation mode. Please refer to the Configuration Register Section and pin description for more detail.

1.2.11.4 Serial Port Interrupt Generation

The LIO.E supports two separate serial ports (i.e., 16450, 16550A) that allow each interrupt source (UARTINTA, UARTINTB) to be assigned to one of the four interrupt outputs (COM1IRQ, COM2IRQ, COM3IRQ, and COM4IRQ). The inputs OUT2A# and OUT2B# provide tri-state control to the selected interrupt output in a PC/AT compatible manner. These interrupts can be assigned as either edge or level compatible based on configuration register C5h. Please refer to the Configuration Register Section and pin description for more detail.

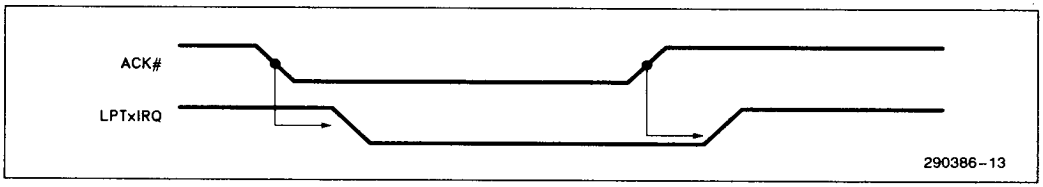


Figure 1-12. Parallel Port Interrupt Generation (Edge Compatible Mode)

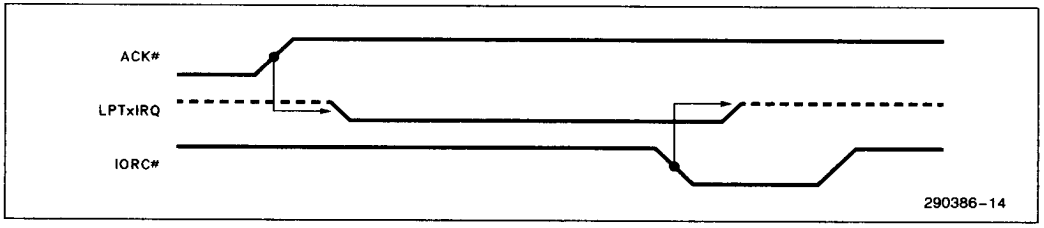


Figure 1-13. Parallel Port Interrupt Generation (Level Compatible Mode)

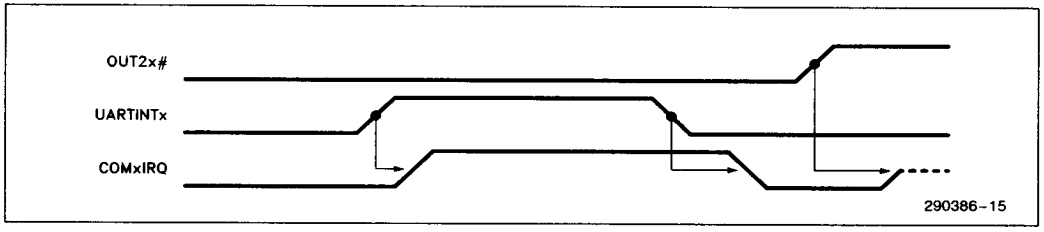


Figure 1-14. Serial Port Interrupt Generation (Edge Compatible Mode)

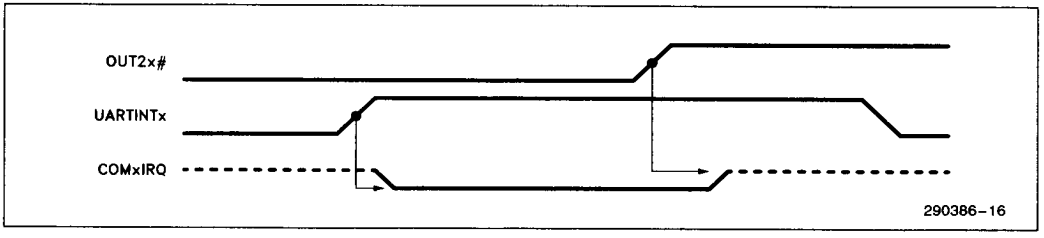


Figure 1-15. Serial Port Interrupt Generation (Level Compatible Mode)

1.2.12 NUMERIC COPROCESSOR INTERFACE

The numeric coprocessor interface block is designed to support either the 80386/80387 combination or the 80486 with its internal numeric coprocessor. The implementation for either mode is designed to be fully PC/AT compatible in the way numeric coprocessor exceptions are reported.

The mode is selected by the state of NPBUSY#/CPUSEL on the trailing edge of RESET. If NPBUSY#/CPUSEL is sampled low, the 80486 mode is enabled.

This interface provides numeric coprocessor data requests to the CPU through CPUPEREQ. It provides indication of data processing by the numerics coprocessor through CPUBUSY#, and if an error is encountered during data processing by the numeric coprocessor, it is indicated to the CPU through IRQ13.

1.2.12.1 80386 Interface

CPUPEREQ and IRQ13 Generation

Whenever the numeric coprocessor generates NPPEREQ, CPUPEREQ is generated by LIO.E.

Whenever the numeric coprocessor encounters an error during computation, it generates NPERROR# when NPBUSY#/CPUSEL is low and generates CUPEREQ, CPUBUSY#, and IRQ13 as shown in the following waveforms. These signals are reset by the falling edge of IOWC# while writing to Register 00F0h.

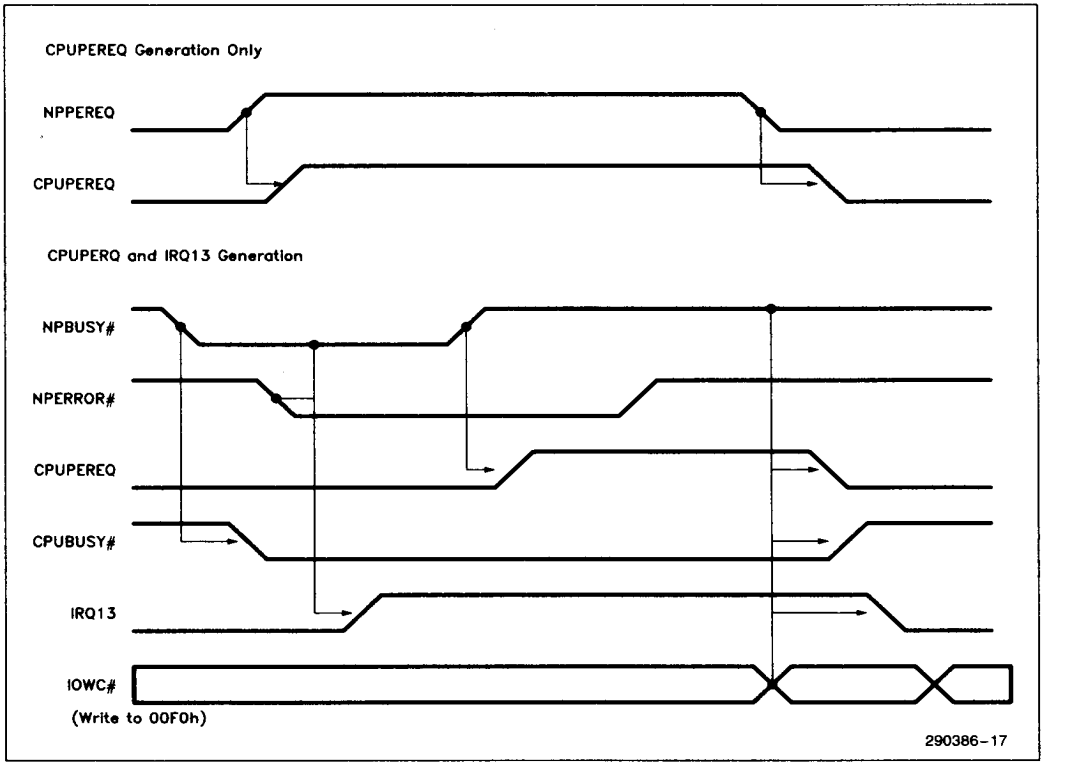


Figure 1-16. CPUPEREQ and IRQ13 Waveforms

CPUBUSY# Generation

CPUBUSY# is generated whenever NPBUSY#/CPUSEL is activated by the Numeric processor, or an active pulse on NPCYCLE# is latched and synchronized to activate CPUBUSY# for at least four BCLKs. This is shown in Figure 1-17 CPUBUSY# Generation.

1.2.12.2 80486 CPU Interface

CPUIGNNE# and IRQ13

Whenever the numeric coprocessor encounters an error during computation, it generates NPERROR#, which causes IRQ13 to be driven active. CPUIGNNE# is generated and IRQ13 is driven inactive during an I/O write to 00F0h. This is shown in Figure 1-18 CPUIGNNE# and IRQ13 Generation.

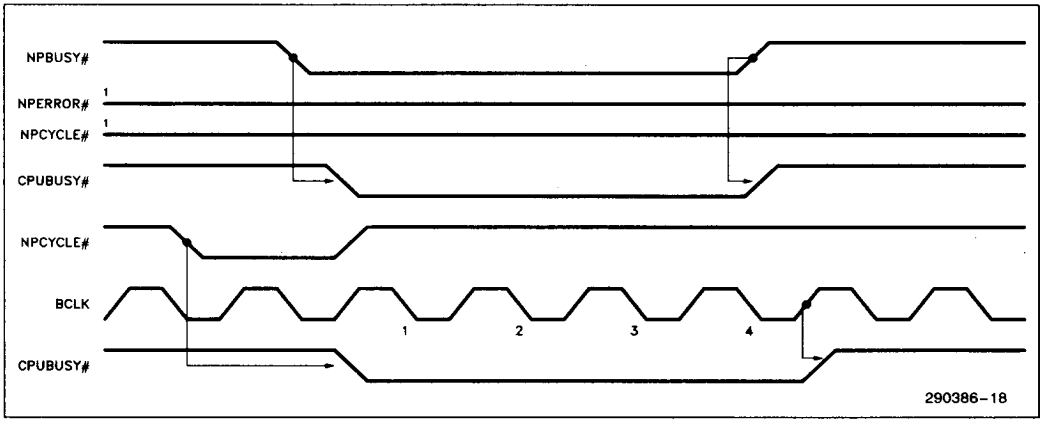


Figure 1-17. CPUBUSY# Generation

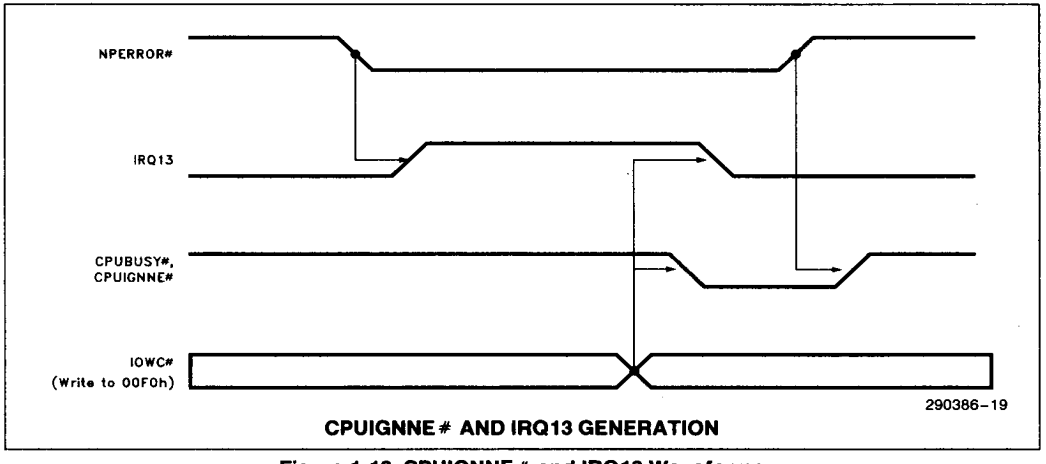


Figure 1-18. CPUIGNNE# and IRQ13 Waveforms

2.0 REGISTER DESCRIPTION

2.1 Configuration Registers

The Configuration Registers can be accessed only by writing the proper ID data (02h) in the ID Register at offset address of 21h. The various interfaces can be initialized or selected by writing into their respective Configuration Registers and other associated Registers which are discussed in detail later.

NOTE:
The LIO.E only can use this ID value, no other device can use this value.

2.1.1 CONFIGURATION REGISTER ACCESS

Configuration Registers of the LIO.E are accessed through an index scheme. An index register that points to the target register is located at 0022H. The target register is accessible at 0023H once the index register is loaded with the desired offset. After every access of location 0023H, the index register is cleared and must be reloaded before another access is allowed. Improper programming sequences are ignored by the LIO.E. For example, if 22h is programmed twice prior to 23h being programmed, the first access to 22h is ignored.

To support multiple peripherals that utilize this index register scheme, the LIO.E configuration registers can not be accessed until the ID register has been properly initialized.

Programming Example: Disable the Floppy Disk Controller

```
        Address    Data

OUT     22h,       21h
OUT     23h,       02h
OUT     22h,       C0h
OUT     23h,       07h
```

All registers default to a known state after RESET goes active, as shown in the Register Summary Table 2-1.

NOTE:
Reserved bits that are marked with "X" should be set to a "0" for writes. The user should not rely on the contents of reserved bits during read. Failure to follow this procedure could cause unexpected results.

Table 2-1. Configuration Register Summary

Configuration Register	Offset Address	Default Value
I.D. Register	21h	00000000b
Peripheral Enable Register A	C0h	xxxx1111b
Peripheral Enable Register B	C1h	10010000b
Parallel Configuration Register	C2h	xxxxx000b
Serial Configuration Register A	C3h	0100xx11b
Floppy Disk Controller Configuration Register	C4h	xxxxx000b
Serial Configuration Register B	C5h	0100xxx0b
COM3 Programmable Chip Select Low Address	C6h	11101xxxb
COM3 Programmable Chip Select High Address	C7h	00000011b
COM4 Programmable Chip Select Low Address	C8h	11101xxxb
COM4 Programmable Chip Select High Address	C9h	00000010b
Programmable Chip Select Mask Register 0-3	D0h-D3h	00000000b
Programmable Chip Select Low Address Reg. 0-3	D4h-D7h	00000000b
Programmable Chip Select High Address Reg. 0-3	D8h-DBh	00000000b
Configuration RAM Page Location Register A	DCh	00000000b
Configuration RAM Page Location Register B	DDh	00001100b
Configuration RAM Command Register	DFh	00001000b
EISA ID Configuration Registers	E8h-EBh	11111111b

2.1.1.1 Register Initialization Requirements

In Table 2-2 is a list of the configuration registers that need initialization before it's corresponding module or interface can be used.

Table 2-2. Register Initialization Requirements

Module and/or Interface	Configuration Register(s)
General Purpose Chip Selects	C1h (Bits 0, 1, 2, 3), D0h: DBh
EISA Configuration RAM	C0h (Bit 0), DCh:DFh
EISA ID Registers	E8h:EBh
Keyboard and/or Mouse Interface	C0h (Bit 2), C1h (Bit 6)
I/O Port 92h	C1h (Bit 5)
ALTRC#, A20GATE, FLUSH# Function	C1h (Bit 4 and 5)
Floppy Disk Interface	C0h (Bit 3), C4h
Real-Time Clock Interface	C0h (Bit 1)
Parallel Port Interface	C2h
Serial Port Interface	C3h, C5h, C6h:C9h

2.1.2 ID REGISTER (r/w)

Offset: 21H

Default: 00000000b

Bits 7–4: Reserved.

Bits 3–0: Identification field. "00000010b" must be written to this field before the LIO.E will respond to any other configuration register access. After a RESET, the configuration registers (except the ID register on writes) are disabled since this field defaults to 00000000b.

NOTE:
In order to avoid contention with similar index register devices, the ID register only responds to read operations if the value loaded is **00000010b**. This value can not be used to identify any device except the LIO.E.

2.1.3 PERIPHERAL ENABLE REGISTER A (r/w)

Offset: C0H

Default: XXXX1111b

Bit 7–4: Reserved.

Bit 3: Floppy Disk Controller Enable. A "1" will enable CS077#, SD07, and include CS077# in the generation of SOE#. The FDC interface must also be enabled by sampling DSKCHG# high on the trailing edge of reset.

Bit 2: Keyboard Controller Enable. A "1" will enable KBDCS# and cause generation of SOE# for the buffer control. If cleared to a "0", these signals will remain inactive.

Bit 1: Real-Time Clock (RTC) Enable. A "1" will enable generation of RTCRD# and RTCWR# for an external RTC. This will also enable SOE# when the external RTC is accessed.

Bit 0: Configuration RAM Enable. A "1" will enable generation of CRAMRD# and CRAMWR# for an external configuration RAM. This will also cause the generation of SOE#.

2.1.4 PERIPHERAL ENABLE REGISTER B (r/w)

Offset: C1H

Default: 10010000b

Bit 7: Mouse Interrupt Mode Select. A "0" will select an edge mode compatible interrupt for MSIRQ (active high). In this mode, MSIRQ is non-shareable. A "1" will select a level compatible interrupt for MSIRQ (active low). In this mode MSIRQ is shareable.

Bit 6: Mouse Interrupt Enable. A "1" will enable MSIRQ from the keyboard controller auxiliary port. A "0" will tri-state MSIRQ.

Bit 5: Control Port A20GATE and ALTRC# Enable. A "1" will enable the A20GATE and ALTRC# functions via a control port located at I/O address 0092H. A "0" will cause accesses to 0092h to be ignored.

Bit 4: Keyboard Scan A20GATE and ALTRC# Enable. A "1" will enable the A20GATE and ALTRC# functions by allowing keyboard controller commands to be intercepted by the LIO.E. If this bit is "0", KBDWR# will go active unconditionally with IOWC#.

Bit 3: General Purpose Chip Select 3 Enable. A "1" will enable the GPCS3# function and SOE# generation for buffer control.

Bit 2: General Purpose Chip Select 2 Enable. A "1" will enable the GPCS2# function and SOE# generation for buffer control.

Bit 1: General Purpose Chip Select 1 Enable. A "1" will enable the GPCS1# function and SOE# generation for buffer control.

Bit 0: General Purpose Chip Select 0 Enable. A "1" will enable the GPCS0# function and SOE# generation for buffer control.

2.1.5 PARALLEL CONFIGURATION REGISTER (r/w)

Offset: C2h

Default: XXXX0000b

Bits 7–4: Reserved.

Bit 3: Parallel Port Interrupt Mode Select. A "0" will select an edge mode compatible interrupt for LPTxIRQ. In this mode, LPTxIRQ is non-shareable. A "1" will select a level mode compatible interrupt for LPTxIRQ. In this mode, LPTxIRQ is shareable.

Bit 2: Parallel Port Bi-Directional Enable. A "1" will enable the direction bit of the parallel port control register that allows for bi-directional capability. A "0" places the parallel port in the output only PC/AT compatible mode.

Bits 1–0: Parallel Port Select.

00: LPT1 Enabled

01: LPT2 Enabled

10: LPT3 Enabled

11: Parallel Port Disabled

If LPT1 is enabled, the parallel port is selected at 03BCH–03BFH and LPT1IRQ is generated from ACK# (when enabled). If LPT2 is enabled, the parallel port is selected at 0378H–037FH and LPT2IRQ is generated from ACK#. If LPT3 is enabled, the parallel port is selected at 0278H–027Fh and LPT2IRQ is generated from ACK#. If the parallel port is disabled, both LPT1IRQ and LPT2IRQ are tri-state and the parallel port registers will not be accessible.

2.1.6 SERIAL CONFIGURATION REGISTER A (r/w)

Offset: C3H

Default: 0100XX11b

Bits 7–6: Serial Port B Address Select.

00: 03F8H–03FFH (COM1)

01: 02F8H–02FFH (COM2)

10: COM3 Programmable Chip Select (COM3)

11: COM4 Programmable Chip Select (COM4)

Bits 5–4: Serial Port A Address Select.

00: 03F8H–03FFH (COM1)

01: 02F8H–02FFH (COM2)

10: COM3 Programmable Chip Select (COM3)

11: COM4 Programmable Chip Select (COM4)

NOTE:

If Serial Port A and B are programmed for the same I/O address, the chip select for Port B will be disabled.

Bits 3–2: Reserved.

Bit 1: Serial Port B Enable. A "0" will enable generation of UARTCSB# for an external serial UART. This also enables the output buffer of the interrupt associated with Serial Port B.

Bit 0: Serial Port A Enable. A "0" will enable generation of UARTCSA# for an external serial UART. This also enables the outut buffer of the interrupt associated with Serial Port A.

2.1.7 FDC CONFIGURATION REGISTER

Offset: C4H

Default: XXXXX000b

Bits 7–3: Reserved.

Bit 2: Register 03F7H Buffer Enable. A "1" will enable XD buffer control to allow an I/O read from 03F7H (or 0377h). The SD07 signal will also be disabled. The DSKCHG# signal will be driven on XD7. This bit should equal "1" if the hard disk controller resides on the XD bus.

A "0" will disable XD buffer control for an I/O read from 03F7h (or 0377h). Instead, only SD07 will be driven.

Bit 1: Extended Register Set Enable. A "1" will enable access to the 82077 status registers at 03F0H and 03F1H (or 370H and 371H) in addition to its standard registers. If this bit is "0", only the PC/AT compatible registers at 03F2H, 03F3H, 03F4H, 03F5H, and 03F7H (or 0372h, 0373h, 0374h, 0375h and 0377h) are accessible.

Bit 0: Floppy Disk Controller Address Select.
0: 03F0H–03F8H (Primary Address)
1: 0370H–0377H (Secondary Address)

Table 2-3. FDC Control Signal States
Floppy Control Signal States for an I/O Read of 03F7h.

CRC42	CS077#	SD07	SOE#	XD7
0	0	$\overline{\text{DSKCHG\#}}$	1	FLOAT
1	0	FLOAT	0	$\overline{\text{DSKCHG\#}}$

2.1.8 SERIAL CONFIGURATION REGISTER B (r/w)

Offset: C5H

Default: 0100XXX0b

Bits 7–6: Serial Port B Interrupt Assignment.
00: COM1IRQ
01: COM2IRQ
10: COM3IRQ
11: COM4IRQ

Bits 5–4: Serial Port A Interrupt Assignment.
00: COM1IRQ
01: COM2IRQ
10: COM3IRQ
11: COM4IRQ

Bits 3–1: Reserved.

Bit 0: SIO Interrupt Mode Select. A "0" will select an edge mode compatible interrupt and a "1" will select a level mode compatible interrupt. In the edge mode, COMxIRQ are non-shareable and in the level mode, COMxIRQ are shareable.

2.1.9 COM3 PROGRAMMABLE CHIP SELECT LOW ADDRESS REGISTER

Offset: C6H

Default: 11101XXXb

Bits 7–3: Low Order Address Bits A7–A3 Respectively. The bit field in this register is compared to the corresponding system address bits for a match in the generation of the internal COM3 chip select signal.

2.1.10 COM3 PROGRAMMABLE CHIP SELECT HIGH ADDRESS REGISTER

Offset: C7H

Default: 00000011b

Bits 7–0: High Order Address Bits A15–A8 Respectively. The bit field in this register is compared to the corresponding system address bits for a match in the generation of the internal COM3 chip select signal.

2.1.11 COM4 PROGRAMMABLE CHIP SELECT LOW ADDRESS REGISTER

Offset: C8H

Default: 11101XXXb

Bits 7–3: Low Order Address Bits A7–A3 Respectively. The bit field in this register is compared to the corresponding system address bits for a match in the generation of the internal COM4 chip select signal.

2.1.12 COM4 PROGRAMMABLE CHIP SELECT HIGH ADDRESS REGISTER

Offset: C9H

Default: 00000010b

Bits 7–0: High Order Address Bits A15–A8 Respectively. The bit field in this register is compared to the corresponding system address bits for a match in the generation of the internal COM4 chip select signal.

2.1.13 PROGRAMMABLE CHIP SELECT MASK REGISTERS 0–3 (r/w)

Offset: D0H (GPCS0#)
D1H (GPCS1#)
D2H (GPCS2#)
D3H (GPCS3#)

Default: 00000000b

Bits 7–0: Low Order Address Mask for A7–A0 Respectively. If a mask register bit is a "1", then the corresponding low order address bit is not compared in the generation of the applicable general purpose chip select signal.

2.1.14 PROGRAMMABLE CHIP SELECT LOW ADDRESS REGISTER 0-3 (r/w)

Offset: D4H (GPCS0#)
D5H (GPCS1#)
D6H (GPCS2#)
D7H (GPCS3#)

Default: 00000000b

Bits 7-0: Low Order Address Bits A7-A0 Respectively. The bit field in this register is compared to the corresponding system address bits for a match in the generation of the applicable GPCSx# signal. The programmable chip select mask register determines which bits in this register are compared.

2.1.15 PROGRAMMED CHIP SELECT HIGH ADDRESS REGISTER 0-3 (r/w)

Offset: D8H (GPCS0#)
D9H (GPCS1#)
DAH (GPCS2#)
DBH (GPCS3#)

Default: 00000000b

Bits 7-0: High Order Address Bits A15-A8 Respectively. The bit field in this register is compared to the corresponding system address bits for a match in the generation of the applicable GPCSx# signal.

2.1.16 CONFIGURATION RAM PAGE LOCATION REGISTER A (r/w)

Offset: DCH

Default: 00000000b

Bits 7-0: Low Order Page Relocation Address Bits A7-A0 Respectively. The value programmed into this register determines the low order I/O address location where the configuration RAM page register can be accessed.

2.1.17 CONFIGURATION RAM PAGE LOCATION REGISTER B (r/w)

Offset: DDH

Default: 00001100b

Bits 7-0: High Order Page Relocation Address Bits A15-A8 Respectively. The value programmed into this register determines the high order I/O address location where the configuration RAM page register can be accessed.

2.1.18 CONFIGURATION RAM COMMAND REGISTER B (r/w)

Offset: DFH

Default: 00001000b

Bits 7-0: High Order Command Relocation Address Bits A15-A8 Respectively. The programmed value in this field determines the high order I/O address of the configuration RAM region accessible by IORC# or IOWC#.

2.1.19 EISA ID CONFIGURATION REGISTERS (r/w)

Offset: E8H-EBH

Default: 11111111b

Bits 7-0: The value programmed into these registers at E8H-EBH are reflected to the EISA ID registers located at 0C80H-0C83H respectively.

Table 2-4. Register Summary

Configuration Register	I/O Location	Default Value
PC/AT AND EISA COMPATIBLE REGISTERS		
Parallel Port		
Data Port	03BCh (LPT1) 0378h, 037Ch (LPT2) 0278h, 027Ch (LPT3)	xxxxxxxxb
Parallel Control	03BEh (LPT1) 037Ah, 037Eh (LPT2) 027Ah, 027Eh (LPT3)	xx000000b
Status Port	03BDh (LPT1) 0379h, 037Dh (LPT2) 0279h, 027Dh (LPT3)	N/A
EISA Configuration		
Configuration RAM Page Register	0C00h	00000000b
Configuration RAM Locations	0800h–08FFh	N/A
EISA ID Register	0C80h–0C83h	11111111b
Floppy Disk Controller		
Digital Output Register	03F2h (Primary FDC) 0372h (Secondary FDC)	xxxx0xxxb
System Control Port		
Alternate A20GATE and Reset Control Port	0092h	00100110b

2.2 PC/AT & EISA Compatible Registers

2.2.1 PARALLEL PORT

2.2.1.1 Data Port (r/w)

Address: 03BCh (LPT1)
0378h, 037Ch (LPT2)
0278h, 027Ch (LPT3)

Default: XXXXXXXXb

In the uni-directional mode (Configuration Register C2h bit 2 = 0), a write operation to the port immediately presents data to PD(7:0). A read operation from this port produces the last data written to it.

In the bi-directional mode (configuration register C2h bit 2 = 1), a write operation latches the data, but the data is only presented on PD(7:0) if the direction bit of the parallel control register is set to 0. A read operation in the bi-directional mode produces the data previously written if the direction bit is 0, or the data on PD(7:0) from potentially another device if the direction bit is 1.

2.2.1.2 Parallel Control (r/w)

Address: 03BEh (LPT1)
037Ah, 037Eh (LPT2)
027Ah, 027Eh (LPT3)

Default: XX000000b

Bits 7–6: Reserved.

Bit 5: Direction. When this bit is a 0, the data port is written to. When this bit is set to 1, the data port is read from. This bit is only writable to a 1 if configuration register C2h bit 2 is a 1.

Bit 4: Interrupt Enable (+). A 1 enables the selected LPTxIRQ signal to go active from the rising edge of the printer control signal ACK#.

Bit 3: Select In (+). This bit controls the SLCTIN# signal. When this bit is a 1, the printer is selected.

Bit 2: Initialize (−). This bit controls the INIT# signal. When this bit is a 0, the printer starts.

Bit 1: Automatic Feed (+). This bit controls the AUTOFD# signal. When this bit is a 1, the printer automatically spaces the paper up one line for every line return.

Bit 0: Strobe (+). This bit controls the STROBE# signal. When this bit is a 1, data is clocked into the printer.

2.2.1.3 Status Port (r)

Address: 03BDh (LPT1)
0379h, 037Dh (LPT2)
0279h, 027Dh (LPT3)

Default: N/A

Bit 7: Busy (−). This bit represents the state of the BUSY signal in complement form. When this bit is a 0, the printer is busy and cannot accept data.

Bit 6: Acknowledge (−). This bit represents the state of the ACK# signal. When this bit is a 0, the printer has received a character and is ready to accept another.

Bit 5: Paper End (+). This bit represents the state of the PE signal. When this bit is a 1, the printer has detected the end of the paper.

Bit 4: Select (+). This bit presents the state of the SLCT signal. When this bit is a 1, the printer has been selected.

Bit 3: Error (−). This bit represents the state of the ERROR# signal. When this bit is a 0, the printer has encountered an error condition.

Bit 2: Interrupt Status (−). If this bit is 0, an interrupt condition is pending.

Bit 1−0: Reserved.

2.2.2 EISA CONFIGURATION

2.2.2.1 Configuration RAM Page Register (r/w)

Address: 0C00H

Default: 00000000b

Bits 7−0: Reserved. The default page size is 256 Bytes.

2.2.2.2 Configuration RAM Locations (r/w)

Address: User Programmable (Default Address = 0800H−08FFH).

Default: N/A

Non-volatile RAM locations available for storing system configuration information in EISA systems. The configuration RAM page register selects a specific segment and the system I/O address SA0−SA7 selects the location within the segment.

2.2.2.3 EISA ID Registers (r)

Address: 0C80H−0C83H

Default: 11111111b

Read-only EISA system ID registers. The EISA compatible system ID contents are programmed into these registers via the configuration registers (see Section 2.1.19) during the initialization of the LIO.E.

2.2.3 FLOPPY DISK CONTROLLER

2.2.3.1 Digital Output Register (w)

Address: 03F2H (Primary)
0372H (Secondary)

Default: XXXX0XXXb

Bits 7−4: Not Used. These bits exist on the 82077 FDC. Refer to the 82077 data sheet for further details.

Bit 3: DMA Enable. When this bit is a 1, the assertion of DACK2# will result in SOE# being asserted. If this bit is 0, DACK2# has no effect on SOE#.This port bit also exists on the 82077 FDC.

Bit 2−0: Not Used. These bits exist on the 82077 FDC. Refer to the 82077 data sheet for further detail.

2.2.4 SYSTEM CONTROL PORTS

2.2.4.1 Alternate A20GATE & Reset Control Port (r/w)

Address: 0092H

Default: 00100110b

This register is only accessible if configuration register C1h bit 5 is a 1.

Bits 7−6: Fixed Disk Activity Light. If either bit is a 1, DLIGHT# will go low. To force DLIGHT# high, both bits must be 0.

Bit 5: Reserved. This bit will always read a 1.

Bit 4: Not used. This bit will always read a 0.

Bit 3: Security RAM Lock. A 1 disables access to the RTC non-volatile memory from 36H to 3FH (RTCRD# or RTCWR# will not go active for an I/O access between 36h and 3Fh). Once this bit is set to a 1, it can not be cleared until RESET goes active. This bit should only be set during the boot process after the system configuration utilities have been executed.

Bit 2: Reserved. This bit will always read a 1.

Bit 1: A20GATE. This bit is directly reflected on the A20GATE signal.

Bit 0: Alternate Reset. Write a 1 to this bit will cause ALTRC# to pulse active low for approximately three to four BCLKs. Before another reset pulse can be generated, this bit must first be written back to a 0.

Register Notes: Reserved bits that are marked with X should be set to a 0 for writes. The user should not rely on the contents of reserved bits during reads. Failure to follow this procedure could cause unexpected results.

3.0 PIN OVERVIEW

The LIO.E is a 132-pin device having total of 124 signal pins, which are shown below:

3.1 Notations Used

I	Input
O	4 mA Output
IO	Input/4 mA Output
OC	4 mA Open Collector Output
HO	24 mA Output
HIO	Input/24 mA Output
HOC	24 mA Open Collector Output
NC	No Connect

1

3.2 Pin Description

Below is a brief description of each pin on the 82351 LIO.E. The following definitions are used in these descriptions:

Table 3-1. Pin Descriptions

Symbol	I/O	Description
3.2.1. SYSTEM BUS INTERFACE		
RESET	I	**RESET:** Initializes the LIO.E to a default state. This signal should be active for a power on reset only.
BCLK	I	**8.25 to 8.33 MHz SYSTEM BUS CLOCK.**
XD(7:0)	I/O	**UTILITY DATA BUS:** XD(7:0) is an input when IOWC# is active and an output when IORC# is active for the purpose of software initialization. In the input mode, XD(7:0) is also used to monitor keyboard controller commands.
SA(15:0)	I	**SYSTEM ADDRESS BUS.**
REFRESH#	I	**SYSTEM REFRESH INDICATOR:** Used by the address decode logic and buffer control logic to ignore the access if REFRESH# is active.
AEN#	I	**ADDRESS ENABLE:** When active low, this signal indicates a DMA cycle is in progress and the address should be ignored for any I/O cycle supported by the LIO.E for the purpose of device select.
BALE	I	**ADDRESS LATCH ENABLE:** The falling edge of this signal latches the level of BIOSCS# and SA(15:0). When BALE is high, BIOSCS# and SA(15:0) are allowed to flow through the LIO.E.
IORC#	I	**SYSTEM BUS I/O READ COMMAND.**
IOWC#	I	**SYSTEM BUS I/O WRITE COMMAND.**
MRDC#	I	**SYSTEM BUS MEMORY READ COMMAND.**
DSLVCS#	I	**DRAM SLAVE INTERFACE CHIP SELECT:** When active, this signal indicates an internal register of the DRAM controller is currently being accessed. This is used for the enabling of the buffer control signal SOE#.

Table 3-1. Pin Descriptions (Continued)

Symbol	I/O	Description
3.2.1. SYSTEM BUS INTERFACE (Continued)		
ISPCS#	I	**ISP CHIP SELECT:** When active,this signal indicates an internal register of the ISP is currently being accessed. This is used for the enabling of the buffer control signal SOE#.
DACK2#	I	**DMA ACKNOWLEDGE CHANNEL #2:** This signal is active for floppy disk controller DMA transfers and enables the buffer control signal SOE# for I/O reads. For SOE# to be enabled by DACK2#, bit 3 of the floppy disk controller DOR register must be set to a 1. If this bit is a 0 DACK2# will have no effect on SOE#.
3.2.2. BUFFER CONTROL AND GENERAL PURPOSE INTERFACE		
XIORC#	O	**UTILITY BUS I/O READ COMMAND:** The leading edge of this signal is generated from a delayed version of the XOE# trailing edge (when IORC# is active) while the trailing edge is generated directly from the IORC# trailing edge.
XMRDC#	O	**UTILITY BUS MEMORY READ COMMAND:** The leading edge of this signal is generated from a delayed version of the XOE# trailing edge (when MRDC# is active) while the trailing edge is generated directly from the MRDC# trailing edge.
GPCS(3:0)#	O	**GENERAL PURPOSE PROGRAMMABLE CHIP SELECTS:** These outputs will go active if the system address falls within the range dictated by the programmable chip select address and mask registers. GPCS(3:0)# generation is qualified by AEN# and REFRESH# inactive.
XOE#	O	**UTILITY DATA BUS OUTPUT ENABLE:** This signal connects directly to the OEBA# pin of a 74F543 that buffers the utility data bus XD(7:0) from the system data bus SD(7:0). When XOE# is active low during I/O writes and DMA I/O write cycles, data is driven from SD(7:0) to XD(7:0). As a default, this signal remains active and is driven inactive only during I/O read, DMA I/O read, and BIOS memory read cycles.
SOE#	O	**SYSTEM DATA BUS BUFFER OUTPUT ENABLE:** This signal connects directly to the OEAB# pin of a 74F543 that buffers the utility data bus XD(7:0) from the system data bus SD(7:0). When SOE# is active low during I/O read, DMA read, and BIOS memory read cycles, data is driven from XD(7:0) to SD(7:0). SOE# remains inactive otherwise.
3.2.3 KEYBOARD CONTROLLER INTERFACE		
KBDCS#	O	**KEYBOARD CONTROLLER CHIP SELECT:** Active low for I/O address 0060H and 0064H.
KBDWR#	O	**KEYBOARD WRITE COMMAND:** Intercepted version of IOWC# to the keyboard controller.
ALTRC#	O	**ALTERNATE CPU RESET:** Active low signal used to reset the CPU under program control. This signal is generated by monitoring I/O write commands to the keyboard controller which normally supports this function.
A20GATE	O	**A20GATE:** Forces A20 of the CPU to "0" when low for support of real mode compatible software. This signal is generated by directly monitoring I/O write commands to the keyboard controller which normally supports this function.
KBFULL	I	**KEYBOARD BUFFER FULL:** Rising edge of this signal indicates the keyboard controller character output buffer is full. IRQ01 will go active when the rising edge of this signal occurs.

Table 3-1. Pin Descriptions (Continued)

Symbol	I/O	Description
3.2.3 KEYBOARD CONTROLLER INTERFACE (Continued)		
ABFULL	I	**AUXILIARY BUFFER FULL:** Rising edge of this signal indicates the keyboard controller auxiliary buffer for the mouse interface is full. MSIRQ will go active when the rising edge of this signal occurs (see system interrupts).
FLUSH#	O	**CACHE FLUSH:** A change in A20GATE will generate an active low pulse on this signal of nominally 2–3 BCLKs in width.
3.2.4. FLOPPY DISK CONTROLLER INTERFACE		
CS077#	O	**CHIP SELECT OF THE 82077 FLOPPY DISK CONTROLLER:** Active for the I/O address range 03F2h, 03F3h, 03F4h, 03F5h and 03F7h (or secondary range of 0372h, 0373h, 0374h, 0375h and 0377h). If the extended register set is enabled by the FDC configuration register C4h bit 1 = 1, CS077# will also be active for 03F0h and 03F1h (or 0370h and 0371h).
DSKCHG#	I	**DISK CHANGE:** This is connected directly to the DSKCHG# signal of the floppy disk drive connector. DSKCHG# must also be sampled high on the trailing edge of reset to enable CS077#, SOE# (as related to the FDC) and SD07 functions. For systems that do not support the FDC by the LIO.E, DSKCHG# should be strapped low.
SD07#	HO	**SYSTEM DATA BUS BIT 7:** This signal is driven with the negated contents of the DSKCHG# signal when an I/O read of address 03F7H is active when the FDC configuration register C4h bit 2 = 0. See the register description for more detail.
DLIGHT# #	O	**FIXED DISK ACTIVITY LIGHT ENABLE:** This signal goes low if either bit 7 or 6 is set to a "1" at I/O port 0092H.
3.2.5. BIOS INTERFACE		
BIOSCS#	I	**BIOS CHIP SELECT:** When active, this signal indicates the system address is for the BIOS ROM. Normally this signal is generated combinatorially from the pipelined EISA LA bus. It is latched internally by the LIO.E on the falling edge of BALE.
LBIOSCS#	O	**LATCHED BIOS CHIP SELECT:** BIOSCS# is transparently latched with the BALE falling edge and qualified with REFRESH# inactive to generate LBIOSCS#.
3.2.6. REAL-TIME CLOCK INTERFACE		
PS	I	**POWER SENSE:** This pin is tied low, to enable RTCRD# and RTCWR#.
RTCRD#	O	**REAL-TIME CLOCK READ COMMAND:** This is an active low output for I/O reads from address 0071H.
RTCWR#	O	**REAL-TIME CLOCK WRITE COMMAND:** This is an active low output for I/O writes to address 0071H.

Table 3-1. Pin Descriptions (Continued)

Symbol	I/O	Description
3.2.7 PARALLEL PORT		
PD(7:0)	HI/O	**PARALLEL PORT DATA.**
STROBE#	HOC	**DATA STROBE:** Active low indicator that PD(7:0) contains valid data.
AUTOFD#	HOC	**AUTOMATIC FEED:** Active low indicator to a printer to generate a line-feed after a carriage return.
INIT#	HOC	**INITIALIZE:** Active low signal to initialize the parallel port device.
SLCTIN#	HOC	**SELECT IN:** Selects the parallel port device when active low.
SLCT	I	**SELECT:** Active high feedback from the parallel port device to indicate that it has been selected.
BUSY	I	**BUSY:** Indicates the parallel port device is busy and cannot accept data when active high.
ERROR#	I	**ERROR:** Active low indicator of an error on the parallel port.
PE	I	**PAPER END:** Active high indicator of a paper out condition by the printer.
ACK#	I	**ACKNOWLEDGE:** When active low indicates the parallel port device has received the data on PD(7:0) and is ready to accept another byte. The rising edge of ACK# is used to activate the selected LPTxIRQ.
3.2.8 SERIAL PORT A INTERFACE		
UARTCSA#	O	**(UARTCSA#) EXTERNAL UART A CHIP SELECT:** The serial configuration register C3h determines the I/O address range in which this signal will go active.
UARTINTA	I	**(UARTINTA) EXTERNAL UART A INTERRUPT REQUEST:** This signal is used to generate the COM port interrupt request (COMxIRQ).
OUT2A#	I	**EXTERNAL UART A INTERRUPT GATE AND MODE SELECT:** This signal provides the tri-state control for COMxIRQ (see system interrupts) when supporting external UART A mode. If OUT2A# is sampled high on the falling edge of Reset, the external UART A mode is enabled and support for an external interrupt and chip select is provided.

Table 3-1. Pin Descriptions (Continued)

Symbol	I/O	Description
3.2.9 SERIAL PORT B INTERFACE		
UARTCSB#	O	**(UARTCSB#) CHIP SELECT:** The serial configuration register C3h determines the I/O address range in which this signal will go active.
UARTINTB	I	**(UARTINTB) EXTERNAL UART B INTERRUPT REQUEST:** This signal generates the COM port interrupt request (COMxIRQ).
OUT2B#	I	**EXTERNAL UART B INTERRUPT GATE AND MODE SELECT:** This signal provides the tri-state control for COMxIRQ (see system interrupts) when supporting external UART B. If OUT2B# is sampled high on the falling edge of Reset, the external UART B mode is enabled and support for an external interrupt and chip select is provided.
3.2.10 CONFIGURATION RAM INTERFACE		
CRAMRD#	O	**CONFIGURATION RAM READ COMMAND:** Active for an I/O read from the address range programmed into the low and high bytes of the Configuration RAM command registers.
CRAMWR#	O	**CONFIGURATION RAM WRITE COMMAND:** Active for an I/O write to the address range programmed into the low and high bytes of the Configuration RAM command registers.
CPA(4:0)	O	**CONFIGURATION RAM PAGE ADDRESS:** Latched from XD(4:0) by an I/O write to the address programmed into the low and high bytes of the Configuration RAM page location registers.
3.2.11 SYSTEM INTERRUPTS		
COM1IRQ	O	**COM1 INTERRUPT REQUEST:** This signal is generated from Serial Port A or Serial Port B as selected by the serial configuration register C5h. See *Register Description* for more details. COM1IRQ is generated from the selected UARTINTx and OUT2x# signals. COM1IRQ is driven from UARTINTx if OUT2x# is low. If OUT2x# is high, COM1IRQ will tri-state.
COM2IRQ	O	**COM2 INTERRUPT REQUEST:** This active high signal is generated from Serial Port A or Serial Port B as selected by the serial configuration register C5h. Once the interrupt source has been selected, the behavior of COM2IRQ is identical to description of COM1IRQ above.
COM3IRQ	I/O	**COM3 INTERRUPT REQUEST:** This active high signal is generated from Serial Port A or Serial Port B as selected by the serial configuration register C5h. Once the interrupt source has been selected, the behavior of COM3IRQ is identical to description of COM1IRQ above.
COM4IRQ	I/O	**COM4 INTERRUPT REQUEST:** This active high signal is generated from Serial Port A or Serial Port B as selected by the serial configuration register C5h. Once the interrupt source has been selected, the behavior of COM4IRQ is identical to description of COM1IRQ above.

Table 3-1. Pin Descriptions (Continued)

Symbol	I/O	Description
3.2.11 SYSTEM INTERRUPTS (Continued)		
LPT1IRQ	O	**LPT1 INTERRUPT REQUEST:** This signal is driven active from the parallel port ACK# signal if LPT1 is selected via the parallel configuration register C2h bits (1:0) = 00 and the interrupt is enabled by setting bit 4 of the parallel control register to a 1. If bit 3 of the parallel configuration register C2h is 0, the edge compatible mode is selected and LPT1IRQ is active high. If bit 3 is 1, the level mode is selected and LPT1IRQ is active low and tri-state when inactive. Upon RESET, this signal is in edge triggered mode, and is tri-stated.
LPT2IRQ	O	**LPT2 INTERRUPT REQUEST:** This signal is driven active from the parallel port ACK# signal if LPT2 or LPT3 is selected via the parallel configuration register C2h bits (1:0) = 01 or 10 and the interrupt is enabled by setting bit 4 of the printer control register to a 1. If bit 3 of the printer configuration register C2h is 0, the edge compatible mode is selected and LPT2IRQ is active high. If bit 3 is 1, the level mode is selected and LPT2IRQ is active low and tri-state when inactive.
MSIRQ	O	**MOUSE INTERRUPT REQUEST:** This signal indicates the rising edge of ABFULL has been detected. It is an open collector active low signal if bit 7 of the peripheral enable register C1h is a 1. If bit 7 is "0", then MSIRQ is active high. The signal is set inactive by an I/O read of the keyboard output buffer located at 0060H. After RESET, MSIRQ is tri-state until enabled by writing a 1 to bit 6 of the Peripheral Enable Register C1h.
IRQ13	O	**NUMERIC COPROCESSOR EXCEPTION:** IRQ13 is driven active high when an error is detected from the numeric coprocessor. This signal goes low upon an I/O write to 00F0H.
IRQ01	O	**KEYBOARD INTERRUPT REQUEST:** This signal goes active high when the rising edge of KBFULL has been detected. The signal is set inactive by an I/O read of the keyboard output buffer located at 0060h.
3.2.12 NUMERIC COPROCESSOR INTERFACE		
NPERROR#	I	**NUMERIC COPROCESSOR ERROR:** In the 80386 CPU mode, this signal is connected to the ERROR# output of the 80387 numerics coprocessor. In the 80486 CPU mode, this signal is connected to FERR# of the 80486 CPU.
NPBUSY#/ CPUSEL	I	**NUMERIC COPROCESSOR BUSY:** In the 80386 CPU mode, this signal is connected to the BUSY# output of the 80387 numerics coprocessor. During RESET, NPBUSY# is also used to determine the mode of the numeric coprocessor interface. In NPBUSY# is high on the trailing edge of RESET, the 80386 CPU mode is selected. If NPBUSY# is low, the 80486 CPU mode is selected.
NPPEREQ	I	**NUMERIC COPROCESSOR EXTENSION REQUEST:** In the 80386 CPU mode, this signal is connected to the PEREQ output of the 80387 numeric coprocessor. In the 80486 mode, this signal should be connected to ground.
NPCYCLE#	I	**NUMERIC COPROCESSOR CYCLE ACTIVE:** In the 80386 CPU mode, this signal should be pulsed when a coprocessor cycle is decoded. In the 80486 CPU mode, this signal should be pulled high.
CPUPEREQ	O	**CPU PROCESSOR EXTENSION REQUEST:** In the 80386 CPU mode, this signal is connected to the PEREQ input of the 80386 CPU. In the 80486 CPU mode, this signal is a no-connect.
CPUBUSY#/ CPUIGNNE#	O	**CPU BUSY:** In the 80386 CPU mode, this signal is connected to the BUSY# input of the 80386 CPU. In the 80486 CPU mode, this signal is connected to IGNNE# of the 80486.

3.3 LIO.E Initialization and Pins State after RESET

The LIO.E is initialized by a reset followed by a write to various internal Registers. The reset is accomplished by holding the RESET signal active for at least 4 BCLKs. The state of output and I/O pins after reset will be as follows:

Table 3-2. Pin States

Pins	State
XD(0:7)	Tri-State (INPUT)
XMRDC#, XIORC#, XOE#, SOE#	High
GPCS(0:3)#, LBIOSCS#	High
KBDCS#, KBDWR#, ALTRC#, FLUSH#	High
A20GATE	High
CS077#, DLIGHT#	High
SD0,7	Tri-State
RTCRD#, RTCWR#	High
PD(0:7)	Output
STROBE#, AUTOFD#, INIT#, SLCTIN#	Tri-State (Open Collector)
UARTCSA#, UARTCSB#	High
CRAMRD#, CRAMWR#	High
CPA(0:4)	Low
IRQ13	Low
MSIRQ, RTCIRQ#, COM1RQ, COM2IRQ, COM3IRQ, COM4IRQ	Tri-State
LPT1IRQ, LPT2IRQ	Tri-State
CPUPEREQ	Low
CPUBUSY#/CPUIGNNE#	High
RESERVED (Pin 93)	Low

Various modules can be enabled upon reset as shown below:

RESET Falling Edge	Enable/Disable Module
DSKCHG# Sampled High	FDC Interface Enabled
NPBUSY#/CPUSEL Sampled LOW	80486 NP Interface Enabled
NPBUSY#/CPUSEL Sampled HIGH	80386 NP Interface Enabled
OUT2A# Sampled HIGH	External UART A Mode Enabled
OUT2B# Sampled HIGH	External UART B Mode Enabled

3.4 82351 LIO.E Pin Assignments

Notations Used:

I Input
O 4 mA Output
IO Input/4 mA Output
OC 4 mA Open Collector Output
HO 24 mA Output
HIO Input/24 mA Output
HOC 24 mA Open Collector Output
NC No Connect

Table 3-3. 82351 Pin Assignments

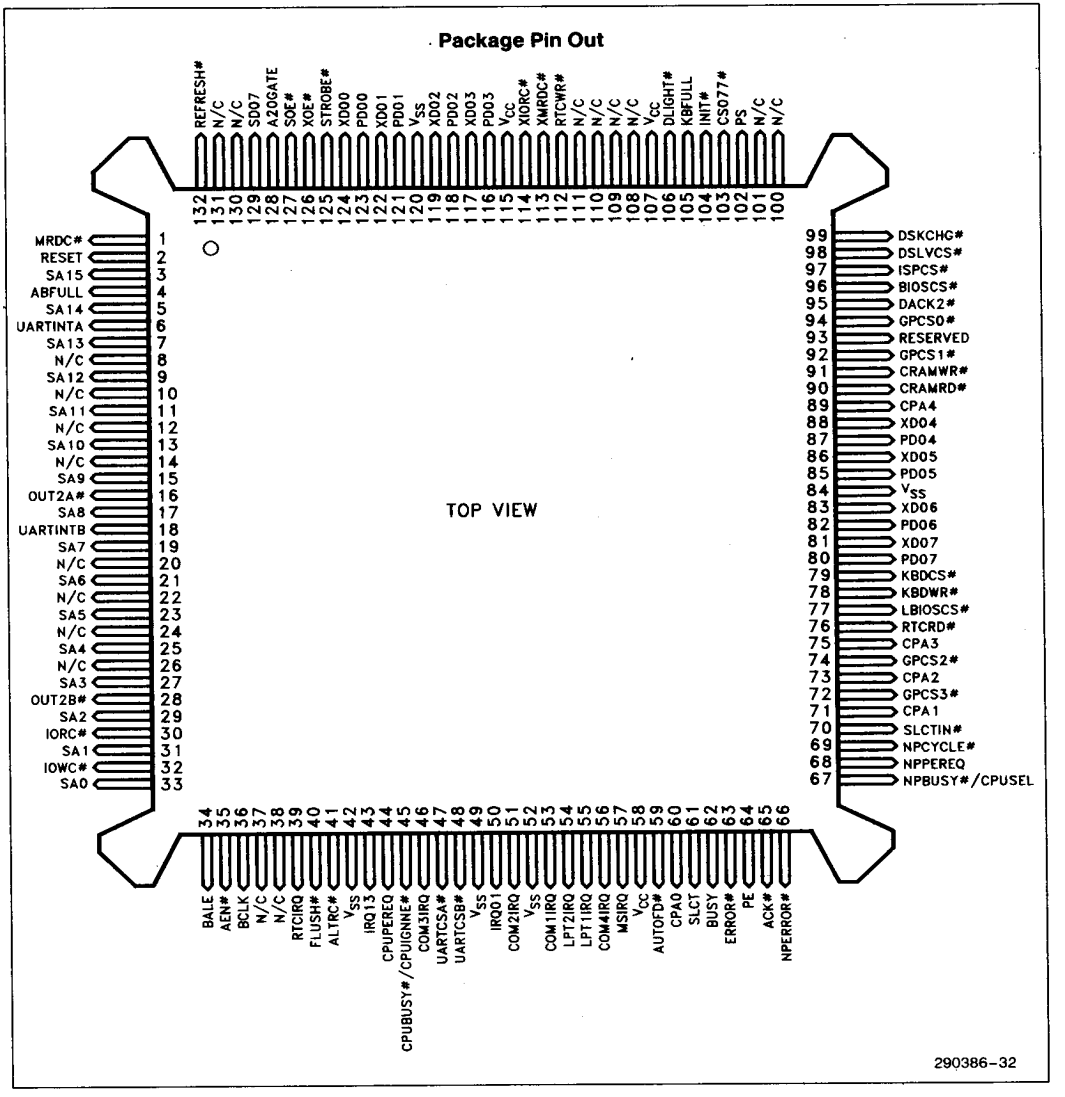
Pin #	Pin Type	Signal Name
1	I	MRDC#
2	I	RESET
3	I	SA15
4	I	ABFULL
5	I	SA14
6	I	UARTINTA
7	I	SA13
8	I	N/C
9	I	SA12
10	I	N/C
11	I	SA11
12	I	N/C
13	I	SA10
14	I	N/C
15	I	SA9
16	I	OUT2A#
17	I	SA8
18	I	UARTINTB
19	I	SA7
20	I	N/C
21	I	SA6
22	I	N/C
23	I	SA5
24	I	N/C
25	I	SA4
26	I	N/C
27	I	SA3
28	I	OUT2B#
29	I	SA2
30	I	IORC#
31	I	SA1
32	I	IOWC#
33	I	SA0
34	I	BALE
35	I	AEN#
36	I	BCLK
37	I	N/C
38	O	N/C
39	OC	RTCIRQ#
40	O	FLUSH#
41	O	ALTRC#
42	I	V_{SS}
43	O	IRQ13
44	O	CPUPEREQ
45	O	CPUBUSY#/CPUIGNNE#
46	O	COM3IRQ
47	O	UARTCSA#
48	O	UARTCSB#
49	I	V_{SS}
50	O	IRQ01
51	O	COM2IRQ
52	I	VSS
53	O	COM1IRQ
54	O	LPT2IRQ
55	O	LPT1IRQ
56	O	COM4IRQ
57	O	MSIRQ
58	I	V_{CC}
59	HOC	AUTOFD#
60	O	CPAO

Table 3-3. 82351 Pin Assignments (Continued)

Pin #	Pin Type	Signal Name
61	I	SLCT
62	I	BUSY
63	I	ERROR#
64	I	PE
65	I	ACK#
66	I	NPERROR#
67	I	NPBUSY#/CPUSEL
68	I	NPPEREQ
69	I	NPCYCLE#
70	HOC	SLCTIN#
71	O	CPA1
72	O	GPCS3#
73	O	CPA2
74	O	GPCS2#
75	O	CPA3
76	O	RTCRD#
77	O	LBIOSCS#
78	O	KBDWR#
79	O	KBDCS#
80	HIO	PD07
81	IO	XD07
82	HIO	PD06
83	IO	XD06
84	I	V_{SS}
85	HIO	PD05
86	IO	XD05
87	HIO	PD04
88	IO	XD04
89	O	CPA4
90	O	CRAMRD#
91	O	CRAMWR#
92	O	GPCS1#
93	O	RESERVED
94	O	GPCS0#
95	I	DACK2#
96	I	BIOSCS#

Pin #	Pin Type	Signal Name
97	I	ISPCS#
98	I	DSLVCS#
99	I	DSKCHG#
100	I	N/C
101	I	N/C
102	I	PS
103	O	CS077#
104	HOC	INIT#
105	I	KBFULL
106	O	DLIGHT#
107	I	V_{CC}
108	O	N/C
109	O	N/C
110	O	N/C
111	O	N/C
112	O	RTCWR#
113	O	XMRDC#
114	O	XIORC#
115	I	V_{CC}
116	HIO	PD03
117	IO	XD03
118	HIO	PD02
119	IO	XD02
120	I	V_{SS}
121	HIO	PD01
122	IO	XD01
123	HIO	PD00
124	IO	XD00
125	HOC	STROBE#
126	O	XOE#
127	O	SOE#
128	O	A20GATE
129	HO	SD07
130	O	N/C
131	I	N/C
132	I	REFRESH#

3.5 82351 LIO.E Pin Out



4.0 ELECTRICAL DATA

4.1 D.C. Specifications

Table 4-1. D.C. Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IL}	Input Low Voltage	−0.5		+0.8	V	—
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	—
V_{OL}	Output Low Voltage	—		0.5	V	1
V_{OH}	Output High Voltage	2.4		—	V	2
I_{CC}	Supply Current	0.5		40	mA	—
I_{IH}	Input Leakage Current	—		±15	μA	—
I_{IL}	Input Leakage Current	—		±15	μA	—
I_{LO}	Output Leakage Current	—		±15	μA	—
C_{IN}	Input Capacitance	—	6	10	pF	3
C_O	I/O or Output Capacitance	—	11	16	pF	3

NOTES:

1. Measured at:

Pin Type	I_{OL}
O	4 mA
IO	4 mA
OC	4 mA
HO	24 mA
HIO	24 mA
HOC	24 mA

2. Measured at:

Pin Type	I_{OH}
O	−1 mA
IO	−1 mA
HO	−4 mA
HIO	−15 mA

3. Sampled only, not 100% tested.

4.2 Absolute Maximum Ratings

Case Temperature under Bias . . . −65°C to +110°C

Storage Temperature . . . . . −65°C to +150°C

Supply Voltages with Respect to Ground . . . . . −0.5V to V_{CC} + 0.5V

Voltage on Any Pin . . . . . −0.5V to V_{CC} + 0.5V

Power Dissipation . . . . . TBD

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.3 A.C. Specifications

A.C. Specifications are based on the following capacitive loading values:
Min specs. = 8 pF cap loading
Max specs. = 50 pF cap loading, except SD07 = 240 pF
NOTE: 0 Minimum Specifications are not Tested, but are Guaranteed by Design.

Table 4-2. A.C. Specifications

Symbol	Parameter	Min	Max	Units	Notes
SYSTEM BUS INTERFACE					
t1	BCLK Period	120		ns	
t2	BCLK High Time	50		ns	
t3	BCLK Low Time	50		ns	
t4	Command Active Time	200		ns	
t5	Command Inactive Time	100		ns	
t6	AEN#, REFRESH#, DACK2# Setup to Command	80		ns	
t7	AEN#, REFRESH#, DACK2# Hold from Command	30		ns	
t8	XD(7:0) Setup to Command (Write)	10		ns	
t9	XD(7:0) Hold from Command (Write)	10		ns	
t10	XD(7:0) Valid from XOE# (Read)	15	150	ns	
t11	XD(7:0) Hold from Command (Read)	0	30	ns	
t12	BIOSCS# Setup to BALE Falling	20		ns	
t13	BIOSCS# Hold from BALE Falling	20		ns	
t14	BALE Pulse Width	30		ns	
t15	SA(15:0) Setup to BALE Falling	20		ns	
t16	SA(15:0) Hold from BALE Falling	20		ns	
t17	BIOSCS# Setup to Command	60		ns	
t18	SA(15:0) Setup to Command	80		ns	
t19	BALE High to Command	80		ns	

Table 4-2. A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Units	Notes
BUFFER CONTROL					
t20	DSLVCS#, ISPCS# Active to SOE# Low		40	ns	14
t21	DSLVCS# ISPCS# Inactive to SOE# High		40	ns	14
t22	IORC#, MRDC# Active to XOE# High	0	25	ns	
t23	XOE# High to XIORC#, XMRDC# Active	22	100	ns	
t24	IORC#, MRDC# Inactive to XIORC#, XMRDC#	0	30	ns	
t25	XIORC#, XMRDC# Inactive to XOE# Low	15	100	ns	
t26	IORC#, MRDC# Active to SOE# Low	0	40	ns	14
t27	IORC#, MRDC# Inactive to SOE# High	0	25	ns	14
DEVICE SELECTS					
t40	SA(15:0), AEN# Valid and BALE High to GPCS(3:0)# Valid	0	60	ns	
t41	SA(15:0), AEN# Valid and BALE High to CS077# Valid	0	60	ns	
t42	SA(15:0), AEN# Valid and BALE High to KBDCS# Valid	0	60	ns	
t43	SA(15:0), AEN# Valid and BALE High to UARTCSA#, UARTCSB# Valid	0	60	ns	
t44	BIOSCS# Valid and BALE High to LBIOSCS# Valid	0	60	ns	
t46	XOE# High to CRAMRD#, RTCRD#, Active	22	100	ns	
t47A	IORC# Inactive to RTCRD# Inactive	0	30	ns	
t47B	IORC# Inactive to CRAMRD# Inactive		40	ns	
t48	IOWC# Setup to BCLK Rising	20		ns	1
t49	IOWC# Hold from BCLK Rising	0		ns	1
t50	IOWC# Active to CRAMWR#, RTCWR# Active	0	50	ns	
t50A	BCLK Falling to KBDWR# Active	0	50	ns	13
t51	BCLK Rising to CRAMWR#, RTCWR# KBDWR#, Inactive		50	ns	2
t52	IOWC# Inactive to CRAMWR#, RTCWR#, KBDWR# Inactive		50	ns	2
t53	IOWC# Active to CPA(4:0) Valid		100	ns	

Table 4-2. A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Units	Notes
SERIAL PORT INTERRUPT CONTROL					
t60	UARTINTA, UARTINTB Valid to COMxIRQ Valid	0	100	ns	17
t61	OUT2A#, OUT2B# High to COMxIRQ Float	0	100	ns	
t62	UARTINTA, UARTINB High to COMxIRQ Low	0	100	ns	18
t63	UARTINTA, UARTINB Low to COMxIRQ Float	0	100	ns	18
KEYBOARD CONTROLLER INTERFACE					
t70	ABFULL Active to MSIRQ Active	0	100	ns	
t71	IORC# Active to MSIRQ Inactive	0	100	ns	
t72	BCLK Falling to A20GATE Valid	0	50	ns	13
t73	FLUSH# Low Time	A	B	ns	12
t74	IOWC# Inactive to ALTRC# Active	0	60	ns	
t75	BCLK Falling to FLUSH# Active		50	ns	13
t76	ALTRC# Low Time	C	D	ns	20
t77	KBFULL Active to IRQ01 Active	0	100	ns	
t78	IORC# Active to IRQ01 Inactive	0	150	ns	
FDC INTERFACE					
t80	IORC# Active to SD07 Driver	0	100	ns	
t81	DSKCHG# Valid to SD07 Valid	0	100	ns	
t82	IORC# Inactive to SD07 Float	0	30	ns	
t83	DLIGHT# Valid from IOWC# Active		100	ns	
PARALLEL PORT INTERFACE					
t90	IOWC# Falling to PD(7:0), STROBE#, AUTOFD#, INIT#, SLCTIN# Valid	0	100	ns	
t91	ACK# to LPT1IRQ, LPT2IRQ Valid	0	100	ns	15
t92	ACK# Rising to LPT1IQ, LPT2IRQ active	0	100	ns	16
t93	IORC# Active to LPT1IRQ, LPT2IRQ Inactive	0	100	ns	16
t94	PD(7:0) Setup to IORC# Active	60		ns	19
t95	PD(7:0) Hold from IORC# Active	60		ns	19
NUMERIC COPROCESSOR INTERFACE (80386 MODE)					
t100	NPBUSY#/CPUSEL Setup to NPERROR# Active	30		ns	
t101	NPBUSY#/CPUSEL Hold from NPERROR# Falling	30		ns	
t102	NPERROR# Valid to IRQ13 Valid	0	100	ns	3
t104	NPBUSY#/CPUSEL Inactive to CPUEREQ Active	0	35	ns	4
t105	NPBUSY#/CPUSEL Low to CPUBUSY# Low	0	35	ns	
t106	NPPEREQ Valid to CPUPEREQ Valid	0	35	ns	
t108	NPCYCLE# Pulse Width	20		ns	

Table 4-2. A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Units	Notes
NUMERIC COPROCESSOR INTERFACE (80386 MODE) (Continued)					
t109	NPCYCLE# Active to CPUBUSY# Active	0	60	ns	
t110	CPUBUSY# Active Time	1	5	ns	5
t111	IOWC# Active to IRQ13Inactive	0	100	ns	6
t112	IOWC# Active to CPUEREQ Active	0	100	ns	7
t113	IOWC# Active to CPUBUSY# Inactive	0	100	ns	8
NUMERIC COPROCESSOR INTERFACE (80486 MODE)					
t120	NPERROR# Active to IRQ13 Active	0	100	ns	
t121	IOWC# Active to IRQ13 Inactive	0	100	ns	
t122	IOWC# Active to CPUIGNNE# Active	0	100	ns	9
t123	NPERROR# Inactive to CPUIGNNE# Inactive	0	100	ns	

NOTES:
1. IOWC# is an asynchronous input. t48 and t49 must be met in order to be recognized in a particular cycle.
2. CRAMWR#, RTCWR# and KBDWR# go inactive after IOWC# is sensed low for 3 BCLK cycles or until IOWC# goes back inactive.
3. t102 only applies if an I/O write to 00F0H has taken place prior to the falling edge of IRQ13.
4. t104 only applies if NPBUSY#/CPUSEL goes high prior to a I/O write to 00F0H.
5. t110 only applies when NPCYCLE# goes active when no 80387 is present.
6. t111 only applies when NPERROR# is high.
7. t112 only applies when NPPEREQ is low.
8. t113 only applies when NPBUSY#/CPUSEL is high and the 80387 is present.
9. t122 only applies when NPERROR# is low.
10. Only applies to BIOSCS# when BALE is high and t12, t13 have been met.
11. Only applies when t20 has been met.
12. The specification notation should read as follows:
    A = 2BCLK − 20 ns
    B = 3BCLK + 30 ns
13. The BCLK falling edge that was preceded by the BCLK rising edge used for sampling IOWC#.
14. SOE# is generated from the worst case of t20 or t26 or t21 and t27.
15. t91 only applies when configured for edge compatible mode.
16. t92 and t93 only apply when configured for level compatible mode.
17. Only applies in edge compatible mode.
18. Only applies in level compatible mode.
19. Required to guarantee t10 and t11.
20. The specification notataion should read as follows:
    C = 3 BCLK − 20 ns
    D = 4 BLKC + 30 ns

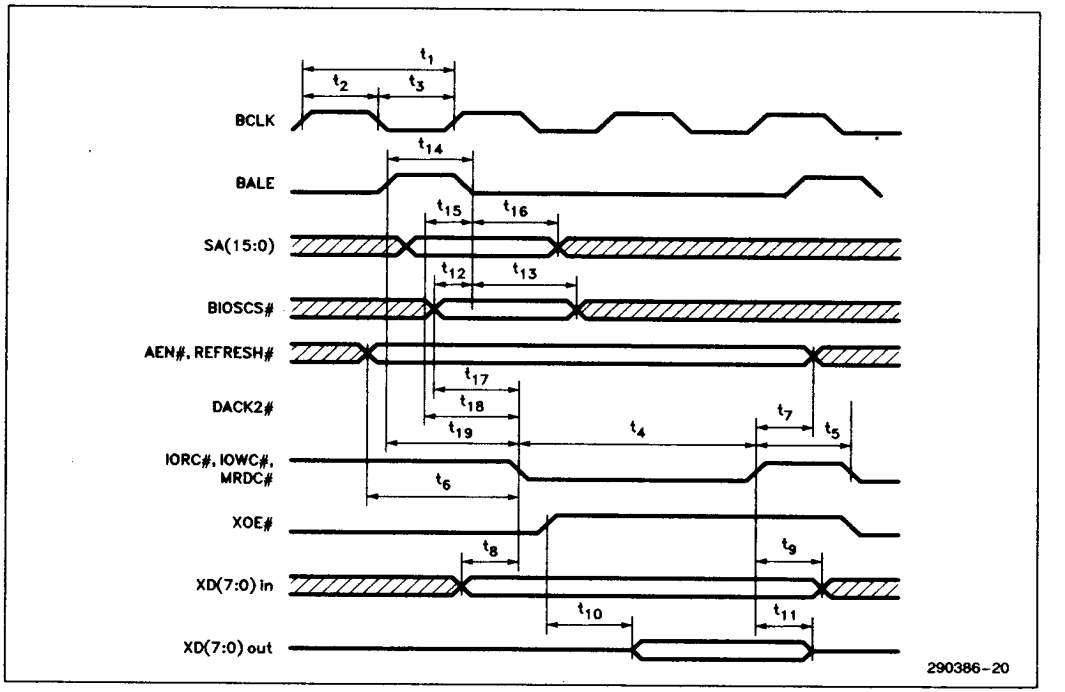


Figure 4-1. System Bus Interface

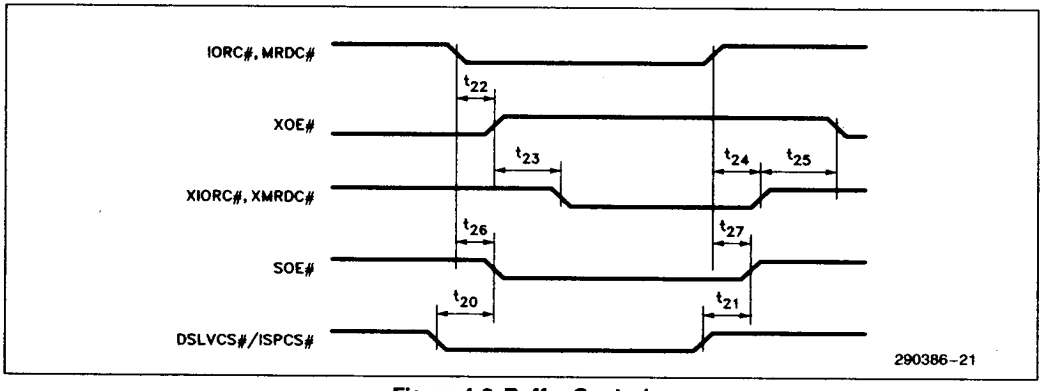


Figure 4-2. Buffer Control

4.4. A.C. Timing Diagrams

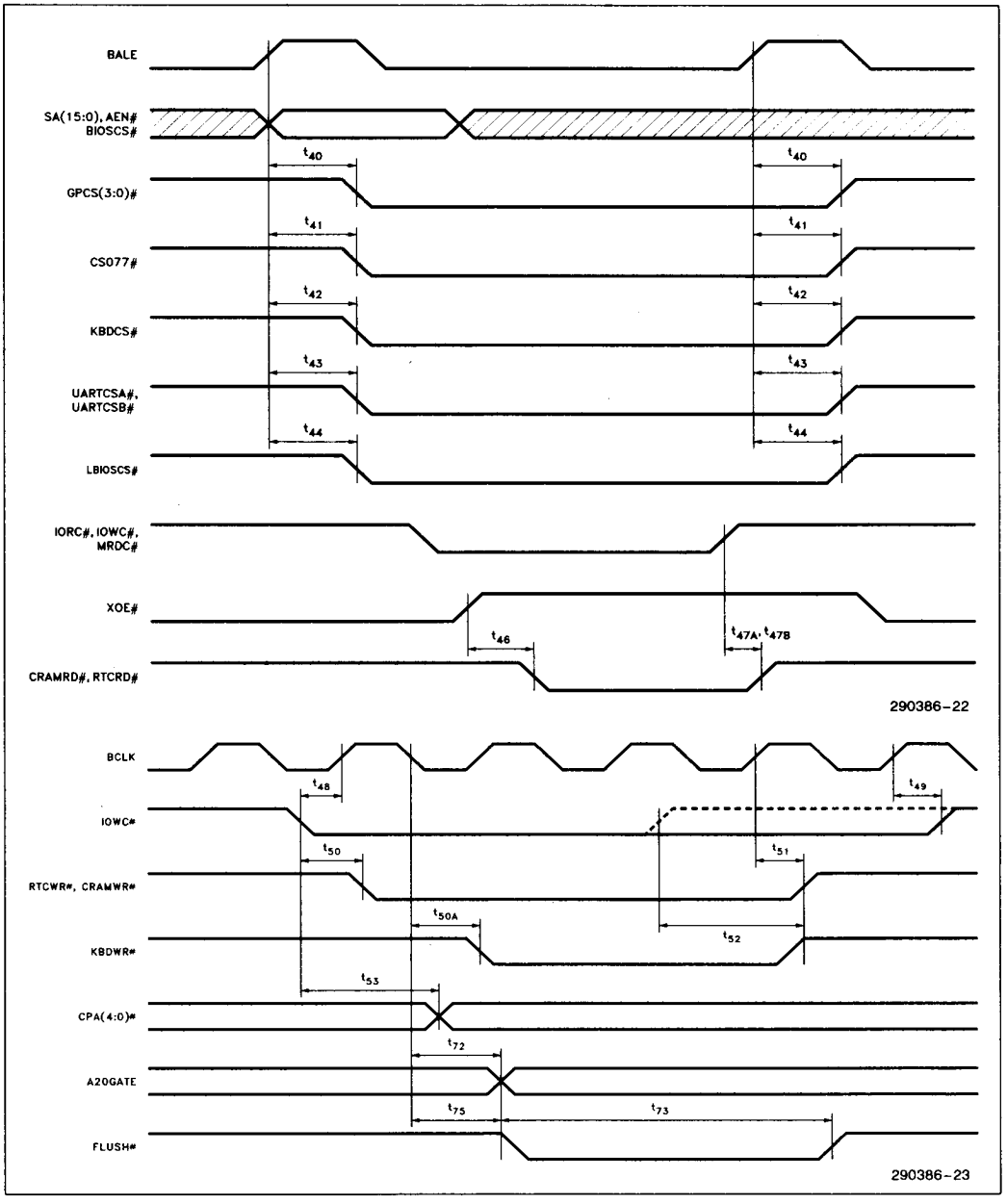


Figure 4-3. Device Selects

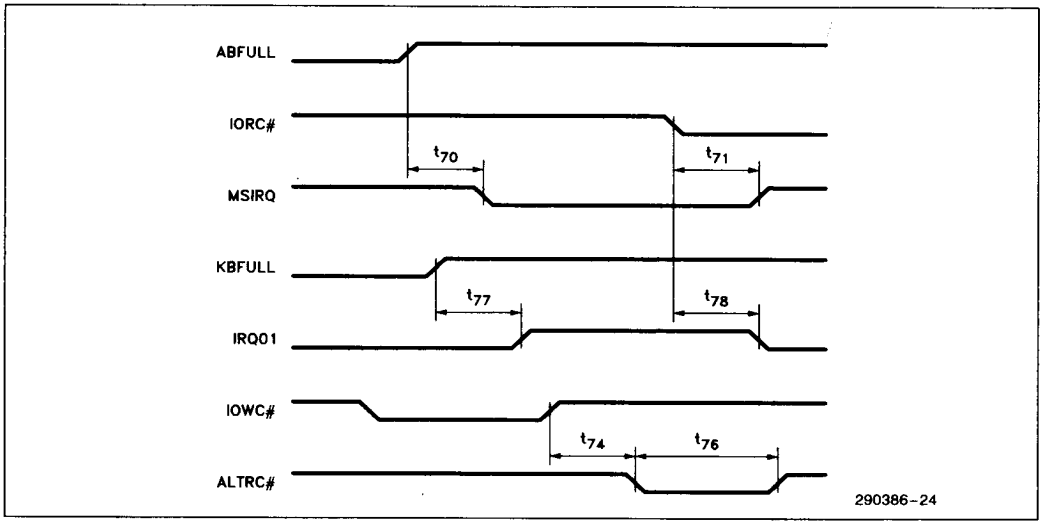


Figure 4-4. Keyboard Controller Interface

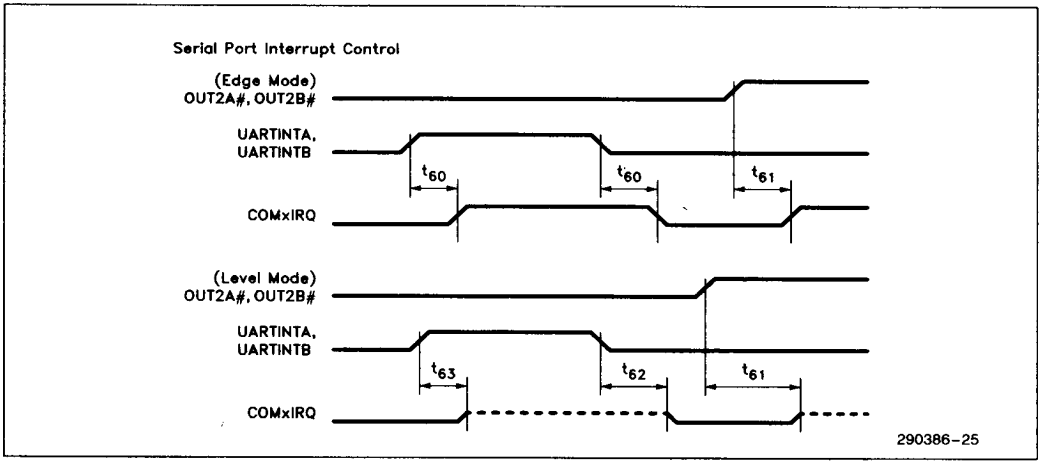


Figure 4-5. Serial Port Interrupt Control

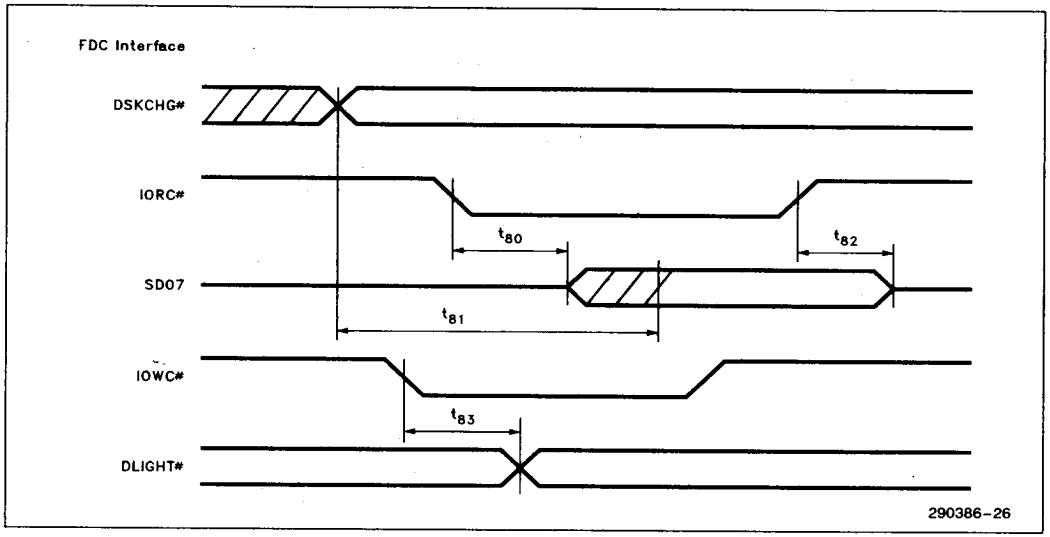


Figure 4-6. FDC Interface

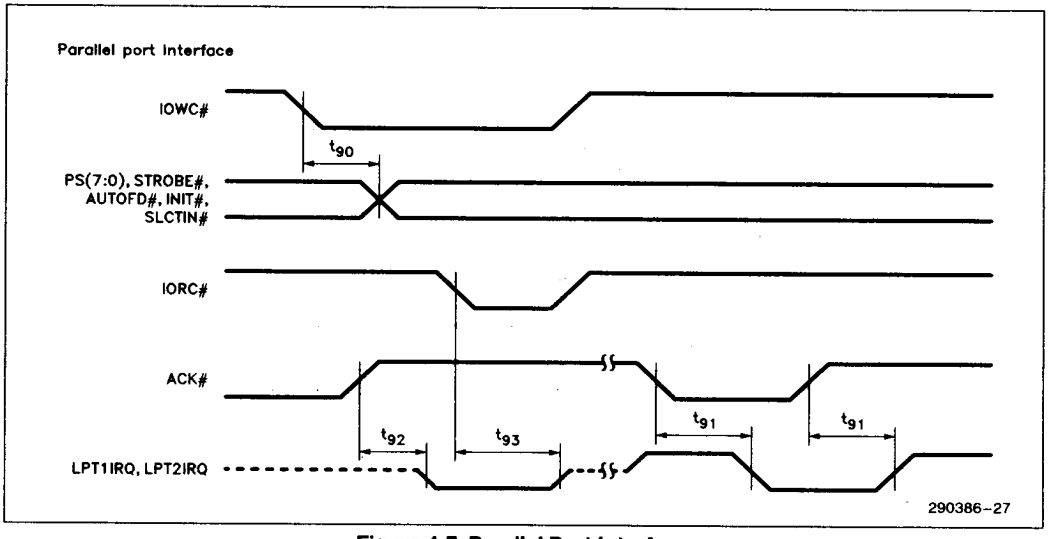


Figure 4-7. Parallel Port Interface

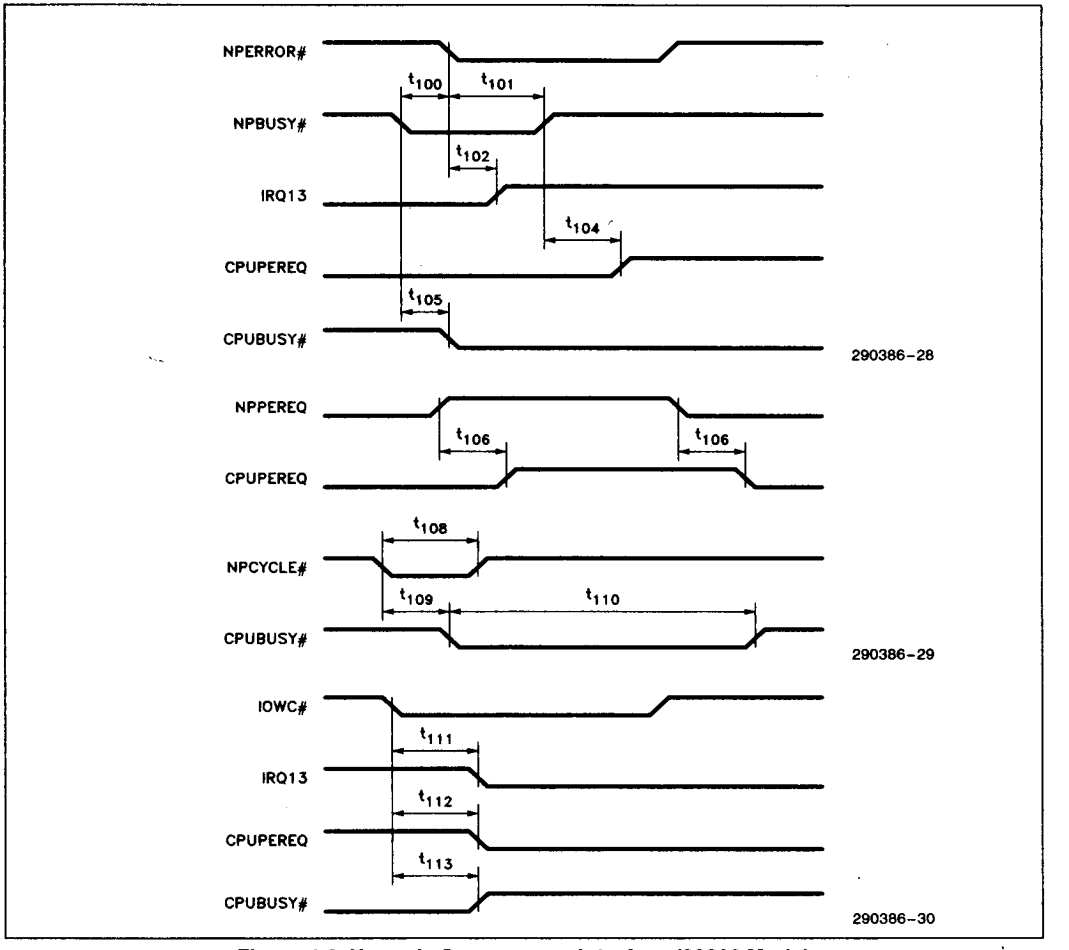


Figure 4-8. Numeric Coprocessor Interface (80386 Mode)

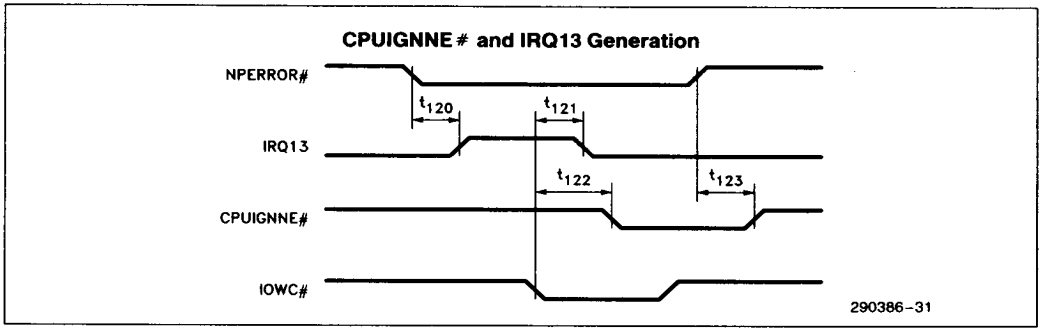


Figure 4-9. Numeric Coprocessor Interface (80486 Mode)

5.0 PACKAGE THERMAL SPECIFICATION

The 82351 LIO.E is specified for operation when the case temperature is within the range of 0°C to +85°C. The case temperature may be measured in any environment, to determine whether the device is within the specified operating range.

The PQFP case temperature should be measured at the center of the top surface opposite the pins, as shown in Figure 5-5 below.

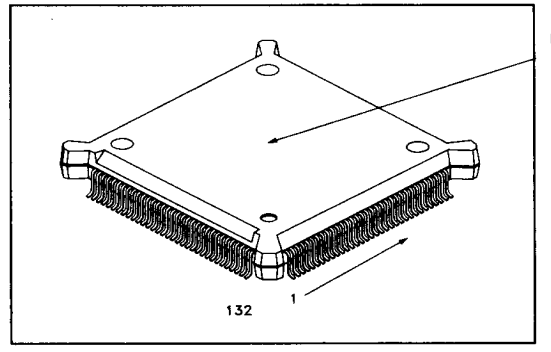


Figure 5-1. Plastic Quad Flat Pack (PQFP)

Table 5-1. 82351 PQFP Package Thermal Characteristics

Thermal Resistance—°C/Watt						
Parameter	**Air Flow Rate (Ft/Min)**					
	0	**200**	**400**	**600**	**800**	**1000**
θ Junction to Case	8	8	8	8	8	8
θ Case to Ambient	32.5	25.5	20	18.5	16	15

NOTES:
1. Table 5-1 applies to 82351 PQFP plugged into a socket or soldered directly into the board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

Process Name: CHMOSIV

Temperature Rise vs. Time:

Time (sec)	**Temperature Rise Unit Power (°C/W)**
0	0
1	3.7
2	6.0
3	7.3
5	9.5

6.0 REVISION SUMMARY

This data sheet contains updates and improvements between version -001 and -002. A revision summary is listed here for your convenience.

82351 Local I/O EISA Support Peripheral (LIO.E)

Section 1.2.5	Changed FLUSH# pulse width to be nominally 2–3 BCLKS duration.
Section 1.2.6	Table 1-3 CS077# Generation, column heading is "DSKCHG#".
Section 1.2.12.1	CPUPEREQ and IRQ13 generation wording was clarified.
Section 1.2.12.2	CPUIGNNE# and IRQ13 generation wording was clarified.
Section 2.1.1	Configuration Command Register (DFh) default value was corrected to 00001000b.
Section 2.1.19	In Table 2.4, Port 92h changed from 00100100b to 00100110b.
Section 2.2.4.1	The default value of Port 92h is 00100110b.
Section 3.2	Revised BCLK description.
Section 3.3	The state of A20GATE after RESET is High.
Section 4.1	V_{OL} maximum is 0.5V. I_{CC} max is 40 mA. Removed I_{LI} spec. Removed notes 4, 5 and 6.
Section 4.3	Minimum Specifications Capacitive loading is 8 pF. Maximum Specifications Capacitive loading is 50 pF, except SD07 = 240 pF Capacitive Loading. t_{25} is 15 ns minimum.

82351 Revision Summary

Version -002 to -003 changes

Section 1.0	Deleted reference to future.
Section 1.2.1	Deleted pins that are not implemented in Figure 1-2.
Section 1.2.3.2	Deleted "DMA" in item number 7.
Section 1.2.10	Deleted 16450 reference.
Section 1.2.11.1	KBDIRQ changed to KBFULL in Figure 1-9.
Section 3.2.6, Section 3.2.8, Section 3.2.9, Section 3.3, and Section 3.4	Deleted pins that are not implemented.
Section 3.5	Added 82351 LIO.E pinout diagram

82351 Revision Summary

The following changes have been made since revision 004:

Section 1.2.5.4	New sentence added to end of paragraph 2. This sentence reads, "The 82351 will latch the last A20GATE value written from either of the above 2 methods.".
Section 1.2.8	New sentence added to paragraph two. This sentence reads, "Note that access is not inhibited on accesses to B6h–BFh which alias to 36h–3Fh.".
Section 2.1.7	New sentence added to Bit 2. This sentence reads, "The DSKCHG# signal will be driven on XD7.".
	New column, "XD7" added to Table 2-3.
Section 3.5	Typo Correction.
Section 4.1	New column, "Typ" added to Table 4-1.
	Added note 3 to Table 4-1.