# 82340-16/20/25MHZ
# 386SX MAIN BOARD

*User's Manual*

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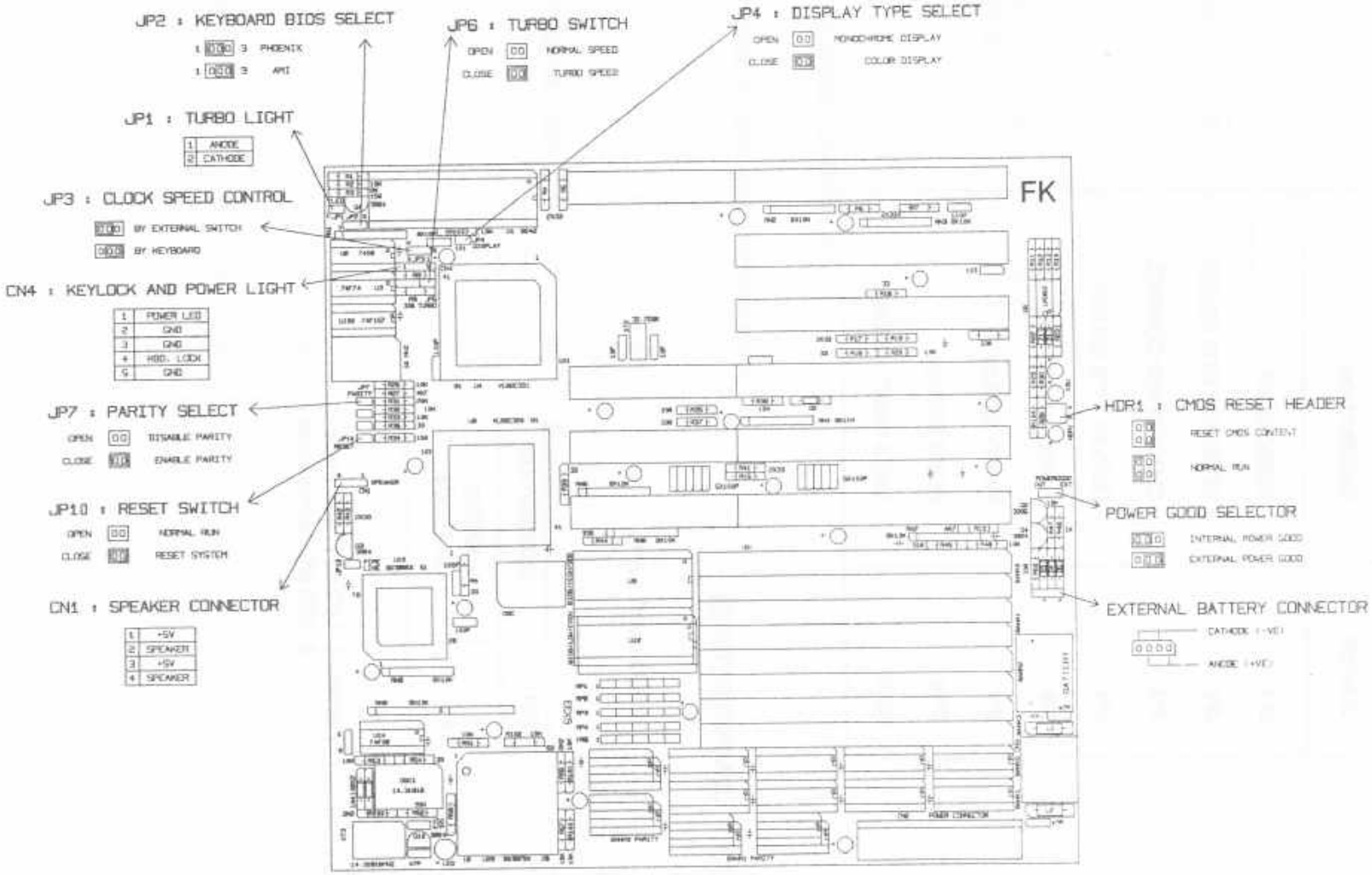
# CHAPTER 1

## GENERAL INFORMATION

The 82340-16/20/25MHZ 386SX MAIN BOARD is a new generation PC/AT compatible main board. It can run at 16/20/25 Mhz clock speed and contains up to 32MB Dram on board. The flexible DRAM combination provides flexibility for the users to choose different combinations of DRAM chips for a specified memory size.

### 1.1 SPECIFICATION

1.) RAM size : maximum 32MB on board
2.) Support 4M x 1 bit and 1M X 4 bits DRAM
3.) Clock speed : 16 / 20 / 25Mhz
4.) Shadow RAM : maximun 384KB size
5.) Support Hardware EMS LIM 4.0
6.) Shadow RAM, EMS and EXTENDED MEMORY can be co-existed with adjustable memory size
7.) Parity can be enabled or disabled
8.) On board power good signal generator
9.) Pre-program DRAM and ROM timing in EPROM BIOS
10.) DRAM access time : 80ns
11.) Fast A20 gate reset
12.) On board rechargeable battery
13.) Support all 286 and 386 programs
14.) 4 x 16 bits slots and 2 x 8 bits slots
15.) 8MHz Bus Clock
16.) Size : 9.3" x 8.7"


JP2 : KEYBOARD BIOS SELECT
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JP6 : TURBO SWITCH
OPEN NORMAL SPEED
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JP4 : DISPLAY TYPE SELECT
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2 CATHODE
JP3 : CLOCK SPEED CONTROL
BY EXTERNAL SWITCH
BY KEYBOARD
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3 GND
4 HDD. LOCK
5 GND
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OPEN NORMAL RUN
CLOSE RESET SYSTEM
CN1 : SPEAKER CONNECTOR
1 +5V
2 SPEAKER
3 +5V
4 SPEAKER
FK
HDR1 : CMOS RESET HEADER
RESET CMOS CONTENT
NORMAL RUN
POWER GOOD SELECTOR
INTERNAL POWER GOOD
EXTERNAL POWER GOOD
EXTERNAL BATTERY CONNECTOR
CATHODE (-VE)
ANODE (+VE)

## 1.3 JUMPER TABLE

| JUMPER | DESCRIPTION |
|---|---|
| JP1 | TURBO LIGHT |
| JP2 | KEYBOARD BIOS SELECT |
| JP3 | CLOCK SPEED CONTROL |
| JP4 | DISPLAY TYPE SELECT |
| JP6 | TURBO SWITCH |
| JP7 | PARITY SELECT |
| JP10 | RESET SWITCH |
| HDR1 | CMOS RESET HEADER |

## 1.4 JUMPER SETTING

### 1.4.1 TURBO LIGHT ( JP1 )

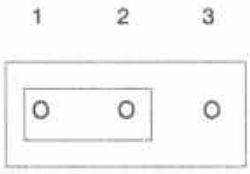
| PIN | DESCRIPTION |
|---|---|
| 1 | + ANODE |
| 2 | - CATHODE |

Notes : 1. LED on ( Turbo mode )
2. LED off ( Normal mode )

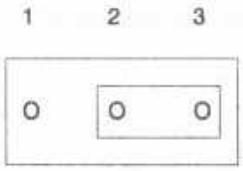
### 1.4.2 KEYBOARD BIOS SELECT ( JP2 )

To select using the Phoenix, AMI, Quadtel and Award BIOS:

Phoenix BIOS



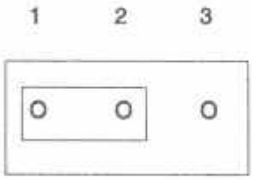

AMI, Quadtel
and Award BIOS



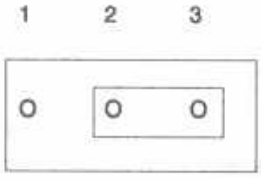

### 1.4.3 CLOCK SPEED CONTROL ( JP3 )

To select the speed by hard switch or software switch:

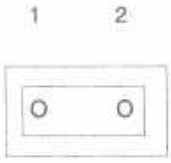
Hard switch/ External switch



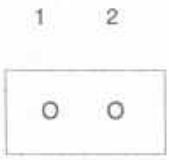

Keyboard switch



### 1.4.4 DISPLAY TYPE SELECT ( JP4 )



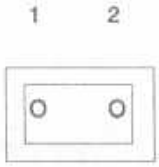

Close = Color Display



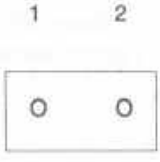

Open = Monochrome Display

### 1.4.5 TURBO SWITCH ( JP6 )

Turbo Named Jumper
=Turbo Switch

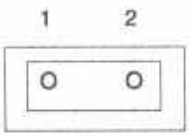



Close = Turbo Speed

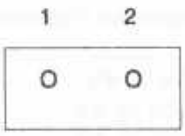



Open = Normal Speed

### 1.4.6 PARITY SELECT ( JP7 )




Close = Parity Enable

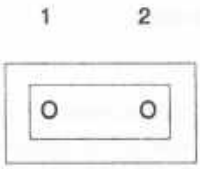



Open = Parity Disable

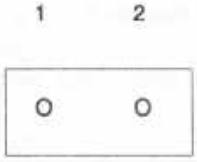
### 1.4.7 RESET SWITCH ( JP10 )

For external reset switch:

Close = Reset

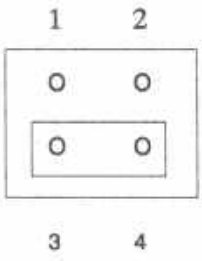



Open = Normal Operation

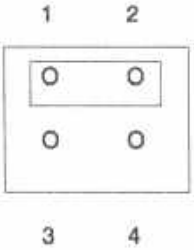



### 1.4.8 CMOS RESET ( HDR1 )

Reset




Run



## 1.5 POWER SUPPLY REQUIREMENT

| Nominal Output | Regulation Tolerance |
|---|---|
| + 5Vdc | +5% to -4% |
| - 5Vdc | +10% to -8% |
| + 12Vdc | +10% to -5% |
| - 12Vdc | +10% to -10% |

## 1.6 PHYSICAL CHARACTERISTICS

* Size: (half baby size) 9.3" x 8.7"
* Mounting holes fit PC/XT, BABY AT or compatible case.

## 1.7 ENVIRONMENT

* Air temperature:
  - System ON : 0 to 45 degrees C (32 to 113 degrees F)
  - System OFF : 10 to 50 degrees C (50 to 122 degrees F)

# CHAPTER2

## INSTALLATION GUIDE

### 2.1 PERIPHERALS REQUIREMENT

1.) 82340-16/20/25MHZ 386SX Main board.
2.) IBM PC/AT power supply or compatible equivalent.
3.) IBM monochrome/graphic display card, color card, EGA or VGA card or compatible.
4.) IBM keyboard or compatible equivalent.
5.) Monochrome or color monitor or VGA monitor.
6.) IBM PC/AT disk drive or compatible equivalent.
7.) IBM HDC/FDC card or compatible equivalent.

### 2.2 PROCEDURES

1.) Connect power supply connectors to CN2 as marked.
2.) Plug in keyboard connector to the keyboard receptical at the back.
3.) Install monochrome or color graphic display card in one of the expansion slots.
4.) Select monochrome or color at JP4.
5.) Connect monitor cable to display card.
6.) This Main Board has a battery but you can plug in the external backup power pack (6V DC) to external battery connector.
7.) Plug in the speaker, reset, turbo, turbo LED and "Power LED and KEYLOCK" connector at the front.
8.) Turn on the monitor.
9.) Turn on the power supply.
10.) Go into the setup mode to set up system configuration.

# CHAPTER 3

## SYSTEM HARDWARE

### 3.1 SYSTEM SPEED

Hardware Speed Control (Turbo Switch JP6)

JP6 Close : Turbo mode
JP6 Open : Non-Turbo mode

### 3.2 HARDWARE RESET (JP10)

JP10 is a hardware reset jumper used to connect a push-button switch.

### 3.3 MONITOR TYPE SELECTION (JP4)

Monochrome: Open PIN 1 and PIN 2.
Color Graphic: Close PIN 1 and PIN2.

## 3.4 SYSTEM MEMORY CONFIGURATIONS

This mainboard must use the same type DRAMs in the same RAM bank pairs, Bank 0, 1 and bank 2, 3 256K DRAMs, or 1M DRAMs, or 4M DRAMs. The RAM speed is 80ns.

| Bank 3 | Bank 2 | Bank 1 | Bank 0 | Total memory size |
|---|---|---|---|---|
| -- | -- | -- | 41256,44256 | 512K |
| -- | -- | 41256,44256 | 41256,44256 | 1M |
| -- | 41256,44256 | 41256,44256 | 41256,44256 | 1.5M |
| 41256,44256 | 41256,44256 | 41256,44256 | 41256,44256 | 2M |
| -- | 1Mx1,1Mx4 | 41256,44256 | 41256,44256 | 3M |
| 1Mx1,1Mx4 | 1Mx1,1Mx4 | 41256,44256 | 41256,44256 | 9M |
| -- | 4Mx1 | 41256,44256 | 41256,44256 | 9M |
| 4Mx1 | 4Mx1 | 41256,44256 | 41256,44256 | 17M |
| -- | -- | -- | 1Mx1,1Mx4 | 2M |
| -- | -- | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 4M |
| -- | 41256,44256 | 1Mx1,1Mx4 | 1Mx1.1Mx4 | 4.5M |
| 41256,44256 | 41256,44256 | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 5M |
| -- | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 6M |
| 1Mx1,1Mx4 | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 8M |
| -- | 4Mx1 | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 12M |
| 4Mx1 | 4Mx1 | 1Mx1,1Mx4 | 1Mx1,1Mx4 | 20M |
| -- | -- | -- | 4Mx1 | 8M |
| -- | -- | 4Mx1 | 4Mx1 | 16M |
| -- | 41256,44256 | 4Mx1 | 4Mx1 | 16.5M |
| 41256,44256 | 41256,44256 | 4Mx1 | 4Mx1 | 17M |
| -- | 1Mx1,1Mx4 | 4Mx1 | 4Mx1 | 18M |
| 1Mx1,1Mx4 | 1Mx1,1Mx4 | 4Mx1 | 4Mx1 | 20M |
| -- | 4Mx1 | 4Mx1 | 4Mx1 | 24M |
| 4Mx1 | 4Mx1 | 4Mx1 | 4Mx1 | 32M |

* Bank 0,1 and Bank 2,3 must have the same DRAM type
* NOTE : BANK 0 AND 1 can used either DIP DRAM or SIMM RAM MODULE and BANK 2 and 3 must use the SIMM RAM MODULE.

## 3.5 POWER SUPPLY CONNECTOR

The pin assignments for the power-supply connectors, PS8 and PS9, are as follows:

| Pin | Assignment | Connector |
|---|---|---|
| 1 | Power good | PS8 |
| 2 | +5 Vdc | |
| 3 | +12 Vdc | |
| 4 | 12 Vdc | |
| 5 | Ground | |
| 6 | Ground | |
| 1 | Ground | PS9 |
| 2 | Ground | |
| 3 | - 5 Vdc | |
| 4 | +5 Vdc | |
| 5 | +5 Vdc | |
| 6 | +5 Vdc | |

## 3.6 KEYBOARD INTERFACE

The CN3 is the keyboard connector, it's a 5-pin DIN connector at the rear of the system board.

The specification is as follow:

| Pin | TTL Signal | Signal Level |
|---|---|---|
| 1 | +Keyboard clock | 5 Vp-p |
| 2 | Keyboard data | 5 Vp-p |
| 3 | N.C. | |
| 4 | Ground | 0 |
| 5 | +5 Volts | +5 Vdc |

## 3.7 POWER LED and KEYLOCK CONNECTOR

The power LED and keylock connector is a 5-pin and its pin assignments as follows:

| Pin | Assignments |
|---|---|
| 1 | LED power |
| 2 | Ground |
| 3 | Ground |
| 4 | Keyboard inhibit |
| 5 | Ground |

## 3.8 SPEAKER INTERFACE

The speaker connection is a 4-pin connector and the pin assignment is as follows:

| Pin | Function |
|---|---|
| 1 | + 5 Vdc |
| 2 | Speaker |
| 3 | + 5 Vdc |
| 4 | Speaker |

## 3.9 EXTERNAL BATTERY CONNECTOR

The external battery connector JP4 is a 4-pin and the pin assignments follow:

| Pin | Assignments |
|---|---|
| 1 | +6 Vdc |
| 2 | Ground |
| 3 | +6 Vdc |
| 4 | Ground |

# CHAPTER 4

# SYSTEM INFORMATION

## 4.1 SYSTEM MEMORY MAP

The system board contains four banks of dynamic RAM with access time of 80 ns. The RAM is parity checked and generate an NMI interrupt if parity error occurs.

| Address Range | MEMORY USAGE | MEMORY STRUCTURE |
|---|---|---|
| 000000 - 07FFFF | 000K - 512K | SYSTEM MEMORY |
| 080000 - 09FFFF | 512K - 640K | SYSTEM MEMORY |
| 0A0000 - 0BFFFF | 640K - 768K | GRAPHIC BUFFER |
| 0C0000 - 0DFFFF | 768K - 896K | EXPANSION ROM |
| 0E0000 - 0EFFFF | 896K - 1.024M | SYSTEM USAGE |
| 100000 - FDFFFF | 1.024M - 16.146M | EXTEND RAM |
| FE0000 - FEFFFF | 16.146M - 16.210M | SYSTEM USAGE |
| FF0000 - FFFFFF | 16.210M - 16.274M | BIOS |

## 4.2 386SX IO ADDDRESS MAP

| Hex Address | Device |
|---|---|
| 000 - 01F | DMA Controller 1 |
| 020 - 03F | Interrupt Controller 1 |
| 040 - 05F | Timer |
| 060 - 06F | Keyboard Controller (8042) |
| 070 - 071 | Real-Time Clock/NMI Mask |
| 080 - 09F | DMA Page Register |
| 0A0 - 0BF | Interrupt Controller 2 |
| 0C0 - 0DF | DMA Controller 2 |
| 0F0 | Clear Math Coprocessor Busy |
| 0F1 | Reset Math Coprocessor |
| 0F8 - 0FF | Math Coprocessor |
| 1F0 - 1F7 | Fixed Disk Controller |
| 200 - 207 | Game I/O |
| 278 - 27F | Parallel Printer Port 2 |
| 2F8 - 2FF | Serial Port 2 |
| 378 - 37F | Parallel printer port 1 |
| 380 - 38F | SDLC, bisynchronous 1 |
| 3A0 - 3AF | Bisynchronous 2 |
| 3B0 - 3BF | Monochrome display, printer adapter |
| 3D0 - 3DF | Color Graphic display adapter |
| 3F0 - 3F7 | Diskette Controller |
| 3F8 - 3FF | Serial Port 1 |

## 4.3 SYSTEM INTERRUPTS

The 80386SX Microprocessor NMI and INT provide 16 levels of system interrupts. The following shows the interrupt-level assignments in decreasing priority.

| Level | Function |
|---|---|
| Micro Processor NMI | Parity or IO Channel Check |
| IRQ 0 | Timer Output 0 |
| IRQ 1 | Keyboard (Output Buffer Full) |
| IRQ 2 | Interrupt from CTLR 2 |
| IRQ 8 | Realtime Clock Interrupt |
| IRQ 9 | Software Redirected to INT 0AH |
| IRQ 10 | Reserved |
| IRQ 11 | Reserved |
| IRQ 12 | Reserved |
| IRQ 13 | Coprocessor |
| IRQ 14 | Fixed Disk Controller |
| IRQ 15 | Reserved |
| IRQ 3 | Serial Port 2 |
| IRQ 4 | Serial Port 1 |
| IRQ 5 | Parallel Port 2 |
| IRQ 6 | Diskette Controller |
| IRQ 7 | Parallel Port 1 |

## 4.4 DMA

The IBM PC-AT supports seven DMA channels, and two INTEL 8237 DMA controller are used. In our system, the equiva lent of two 8237A DMA controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. The DMA channels are assigned as follows:

| DMA CONTROLLER OF VL82C331 | |
|---|---|
| Ctrl 1 | Ctrl 2 |
| Ch0 - Spare | Ch4 - Cascade for Ctrl 1 |
| Ch1 - SDLC | Ch5 - Spare |
| Ch2 - Diskette | Ch6 - Spare |
| Ch3 - Spare | Ch7 - Spare |

DMA channels

DMA controller 1 contains channels 0 through 3. These channels support 8-bit data transfers between 8-bit I/O adapters and 8 or 16-bit system memory. Each channel can transfer data throughout the 16-megabyte system address space in 64KB Blocks. DMA controller 2 contains channels 4 through 7. Channels 5, 6 and 7 support 16-bit data transfers between 16-bit I/O adapters and 16-bit system memory. These DMA channels can transfer data throughout the 16-megabyte system address space in 128 KB blocks. Channels 5, 6 and 7 cannot transfer data on odd byte boundaries.

The following figure shows the address for the page register.

| Page Register | IO Hex Address |
|---|---|
| DMA Channel 0 | 0087 |
| DMA Channel 1 | 0083 |
| DMA Channel 2 | 0081 |
| DMA Channel 3 | 0082 |
| DMA Channel 5 | 008B |
| DMA Channel 6 | 0089 |
| DMA Channel 7 | 008A |
| Refresh | 008F |

Page Register Address

The following figures show address generation for the DMA channels.

| Source | DMA Page Registers | Ctrl 1 |
|---|---|---|
| Address | A23.....A16 | A15.....A0 |

Address Generation for DMA Channels 3 through 0

Note: The addressing signal, 'byte high enable' (BHE), is generated by inverting address line A0.

| Source | DMA Page Registers | Ctrl 2 |
|---|---|---|
| Address | A23.....A17 | A16.....A1 |

Address Generation for DMA Channels 7 through 5

Note: The addressing signal, 'BHE' and 'A0', are forced to logic 0.

## 4.5 SYSTEM COUNTER / TIMER

The 386SX mainboard has 3 programmable timer counter controlled by VL82C331 chip.

# CHAPTER5

## I O CHANNELS

### 5.1 INPUT / OUTPUT SLOTS PINS ASSIGNMENT

The following figure shows the location and the numbering of the IO channel connectors. These connectors consist of six 62-pin and four 36-pin edge connector sockets.

36 PINS SLOT

| | | | | | |
|---|---|---|---|---|---|
| -MEM CS16 | | D1 | C1 | | SBHE |
| -I/O CS16 | | D2 | C2 | | LA23 |
| IR 10 | | D3 | C3 | | LA22 |
| IR 11 | | D4 | C4 | | LA21 |
| IR 12 | | D5 | C5 | | LA20 |
| IR 15 | | D6 | C6 | | LA19 |
| IR 14 | | D7 | C7 | | LA18 |
| -DACK 0 | | D8 | C8 | | LA17 |
| DRQ 0 | | D9 | C9 | | -MEMR |
| -DACK 5 | | D10 | C10 | | -MEMW |
| DRQ 5 | | D11 | C11 | | SD08 |
| -DACK 6 | | D12 | C12 | | SD09 |
| DRQ 6 | | D13 | C13 | | SD10 |
| -DACK 7 | | D14 | C14 | | SD11 |
| DRQ 7 | | D15 | C15 | | SD12 |
| +5V | | D16 | C16 | | SD13 |
| -MASTER | | D17 | C17 | | SD14 |
| GND | | D18 | C18 | | SD15 |

I/O CHANNEL PIN NUMBERING

62 PINS SLOT

| | | | | | |
|---|---|---|---|---|---|
| GND | | B1 | A1 | | -I/O CH CK |
| RESET DRV | | B2 | A2 | | SD07 |
| +5V | | B3 | A3 | | SD06 |
| IR 9 | | B4 | A4 | | SD05 |
| -5V | | B5 | A5 | | SD04 |
| DRQ 2 | | B6 | A6 | | SD03 |
| -12 | | B7 | A7 | | SD02 |
| 0WS | | B8 | A8 | | SD01 |
| +12V | | B9 | A9 | | SD00 |
| GND | | B10 | A10 | | -I/O CH RDY |
| -S MEMW | | B11 | A11 | | AEN |
| -S MEMR | | B12 | A12 | | SA19 |
| -IOW | | B13 | A13 | | SA18 |
| -IOR | | B14 | A14 | | SA17 |
| -DACK 3 | | B15 | A15 | | SA16 |
| DRQ 3 | | B16 | A16 | | SA15 |
| -DACK 1 | | B17 | A17 | | SA14 |
| DRQ 1 | | B18 | A18 | | SA13 |
| -REFRESH | | B19 | A19 | | SA12 |
| SYSCLK | | B20 | A20 | | SA11 |
| IR 7 | | B21 | A21 | | SA10 |
| IR 6 | | B22 | A22 | | SA09 |
| IR 5 | | B23 | A23 | | SA08 |
| IR 4 | | B24 | A24 | | SA07 |
| IR 3 | | B25 | A25 | | SA06 |
| -DACK 2 | | B26 | A26 | | SA05 |
| T/C | | B27 | A27 | | SA04 |
| BALE | | B28 | A28 | | SA03 |
| +5V | | B29 | A29 | | SA02 |
| OSC | | B30 | A30 | | SA01 |
| GND | | B31 | A31 | | SA00 |

## 5.2 I / O Channel Signal Description

All signal lines are TTL- compatible with a maximum loading of two loe-power (LS) deices.

**RESET DRV ( Output )**
The signal goes high during power-up, low line-voltage, or hardware reset.

**SA-19 ( INPUT / OUTPUT )**
The system Address Lines run from bits 0 to 19. They are latched on to the falling edge of " BALE ".

**LA17-23 ( INPUT / OUTPUT )**
The unlatched address liness run from bit 17 to 23.

**SD0-15 ( INPUT / OUTPUT )**
System data bits 0 to 15.

**BALE ( OUTPUT )**
The Buffered - address Latch enable is used to latch SA0-19 on the falling edge. This signal is forced high during DMA cycles.

**I/O CHCK ( Input )**
The I/O Channel Check is an active low signal which indicates that a parity error exists in I/O board.

**I / O CHRDY ( Input )**
This signal lengthens the I/O or memory read/write cycle and should be held low with balid address. It can only be held low for a maximum of 2.5 microseconds.

**IR3-7, 9-12, 14-15 ( Input )**
The Interrupt Request signals which indicate IO service request attention. They are prioritized in the following sequences: HIGHEST IRQ9, 10, 11, 12, 14, 15, 3, 4, 5, 6, 7 Lowest.

**-IOR ( Input / Output )**
The I/O Read Signal is an active low signal which instructs the I/O device to drive its data onto the data bus.

**-IOW ( Input / Output )**
The I/O write is an active low signal which instructs the I/O device to read data from the data bus.

**-SMEMR ( Output )**
The System Memory Read is low while the low 1 mega byte of memory is being used.

**-MEMR ( Input / Output )**
The Memory Read Signal is low while any memory location is being read.

**-SMEMW ( Output )**
The System Memory Write is low while the low 1 mega byte of memory is being used.

**-MEMW ( Input / Output )**
Memory Write is low while any memory location is being written.

**DRQ 0-3, 5-7 ( Input )**
DMA Request channel 0 to 3 are for 8-bit data transfer.
DMA Request channel 5 to 7 are for 16-bit data transfer.
DMA Request channel 4 is used internally on the system board.
DMA Request should be held high until the corresponding DMA.
Their priority is in the following sequence:
Highest DRQ0, 1, 2, 3, 4, 5, 6, 7 Lowest.

**-DACK 0-3, 5-7 ( Output )**
The DMA Acknowledge 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3, 5-7.

**AEN ( Output )**
The DMA Address Enable is high when the DMA controller is driving the address bus.
It is low when the 80286 CPU is driving the address bus.

**-REFRESH ( Input/Output )**
This signal is to indicate that the memory refresh cycle is in progress.

**T/C (Output)**
Terminal Count provides a pulse when the terminal count for any DMA channel is reached.

**SBHE ( Input / Outpu t)**
The System Bus High Enable indicates high byte SD8-15 is on the data bus.

**-MASTER ( Input )**
The Master is the signal from the I/O processor which gains control as the master and it should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh.

**-MEM CS16 ( Input, Open collector )**
The Memory chip Select 16 indicates that the present data transfer is a 1 Wait State 16-bit data memory operation.

**-IO CS16 ( Input, Open collector )**
The I/O Chip Select indicates the present data transfer is a 1-Wait State 16-bit data I/O operation.

**OSC ( Output )**
The Oscillator is a 14.3181 MHz signal used for the color graphic board.

**OWS ( Input, Open collector )**
The 0 Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.